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E.C. NO.	DATE	SHEETS AFFECTED	E.C. NO.	DATE	SHEETS AFFECTED
408296	4-1-64	PAGES 0 THROUGH 88			
408319	6-1-64	3-8,74,80-82,85,86,88			
408319A	7-16-64	4			

CONTENT OF ILD

SECTIONS 01.XX, 02.XX, 05.XX AND 07.XX ARE SELF-EXPLANATORY

SECTIONS 03.XX AND 04.XX CONTAIN OPERATIONALLY ORIENTED FLOW CHARTS COVERING ALL 1620-1311 FUNCTIONS. PAGE 03.01 (OF SECTION 03.XX) CONTAINS AN OVERALL PICTURE OF ALL FILE OPERATIONS AND SERVES AS A PICTURE INDEX TO BOTH SECTIONS 03.XX AND 04.XX. THIS PAGE IS MADE UP OF BLOCKS REPRESENTING MACHINE SUB-OPERATIONS, OR OPERATIONAL UNITS. EACH OF THE REMAINING PAGES OF SECTION 03.XX COVERS A SPECIFIC FILE OPERATION AND CONTAINS ONLY THOSE BLOCKS INVOLVED WITH THAT PARTICULAR OPERATION.

EACH BLOCK ON PAGE 03.01 REPRESENTS A PAGE IN SECTION 04.XX WHICH COVERS A PARTICULAR OPERATIONAL UNIT IN DETAIL.

IN GENERAL, SECTION 03.XX PROVIDES THE VARIOUS COMBINATIONS OF THE BASIC FUNCTION BLOCKS NEEDED TO FOLLOW ANY 1311 OPERATION DESIRED.

SECTION 05.XX CONTAINS A TIMING CHART FOR EACH OPERATIONAL UNIT IN SECTION 04.XX; THESE TWO SECTIONS ARE MATCHED PAGE FOR PAGE.

INTERPRETING THE FLOW CHARTS

WHEN USING THE FLOW CHARTS IN SECTIONS 03.XX AND 04.XX, NOTE, THAT ADJACENT BLOCKS ON ANY ONE PAGE ARE NOT NECESSARILY FUNCTIONALLY RELATED: (E.G., A FUNCTIONAL RELATIONSHIP EXISTS WHEN "A" CAUSES "B" WHICH CAUSES "C", ETC.). THESE CHARTS ARE DESIGNED TO PROVIDE RAPID RECALL BY SHOWING "WHAT HAPPENS" DURING EACH PHASE OF AN OPERATION. IN ORDER TO MEET THIS OBJECTIVE, THE ADJACENT BLOCKS ARE GIVEN A GENERAL TIMING RELATIONSHIP.

MANY FUNCTIONS THAT OCCUR SIMULTANEOUSLY ARE SHOWN IN SERIES TO FACILITATE RAPID READING.

CHANGES AT C SUFFIX

THIS ILD WAS WRITTEN FOR THE C SUFFIX 1311-3, THEREFORE, ALLOWANCE MUST BE MADE WHEN APPLYING THIS INFORMATION TO EARLIER SUFFIXES. THE FOLLOWING CHANGES HAVE BEEN MADE AT THE C SUFFIX LEVEL: THE CLOCK HAS A SINGLE OSCILLATOR; THE INDEX LOCK FEATURE HAS BEEN INCORPORATED ON THE COMPARE DISABLE SWITCH; SEVERAL NEW C.E. AID FEATURES HAVE BEEN ADDED -- THESE ARE COVERED IN DETAIL IN SECTION 07.XX.

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1311 MODEL 3 AND 2 (SATELLITE)
INSTALLATION PROCEDURE

A. UNPACKING AND MACHINE LOCATION

- 1. REMOVE PACKAGING AS PER THE PACK/UNPACK INSTRUCTIONS TAPED TO THE TOP OF THE UNITS AND INSPECT EACH UNIT FOR PHYSICAL DAMAGE. INVENTORY THE PARTS IN THE SHIPPING GROUP AGAINST THE SHIPPING CHECK LIST.
- 2. PLACE DISK STORAGE UNITS IN PROPER POSITIONS (SEE FIGURE 1).
- 3. CHECK THAT SECTOR BLOCK FULLY RETRACTS WHEN COVER IS RAISED.
- 4. REMOVE MACHINE COVERS.
- 5. REMOVE SHIPPING BRACES FROM GATES, ETC.

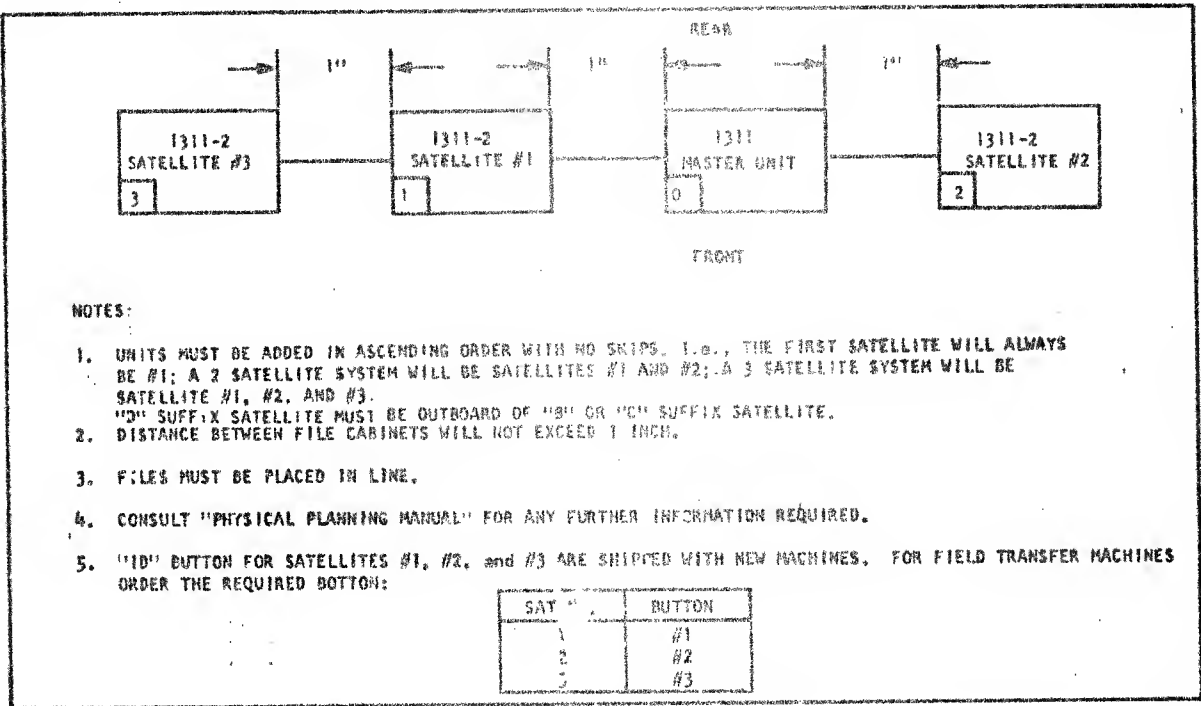


FIGURE 1. SATELLITE PHYSICAL PLACEMENT REQUIREMENTS.

B. CABLING TO PROCESSOR

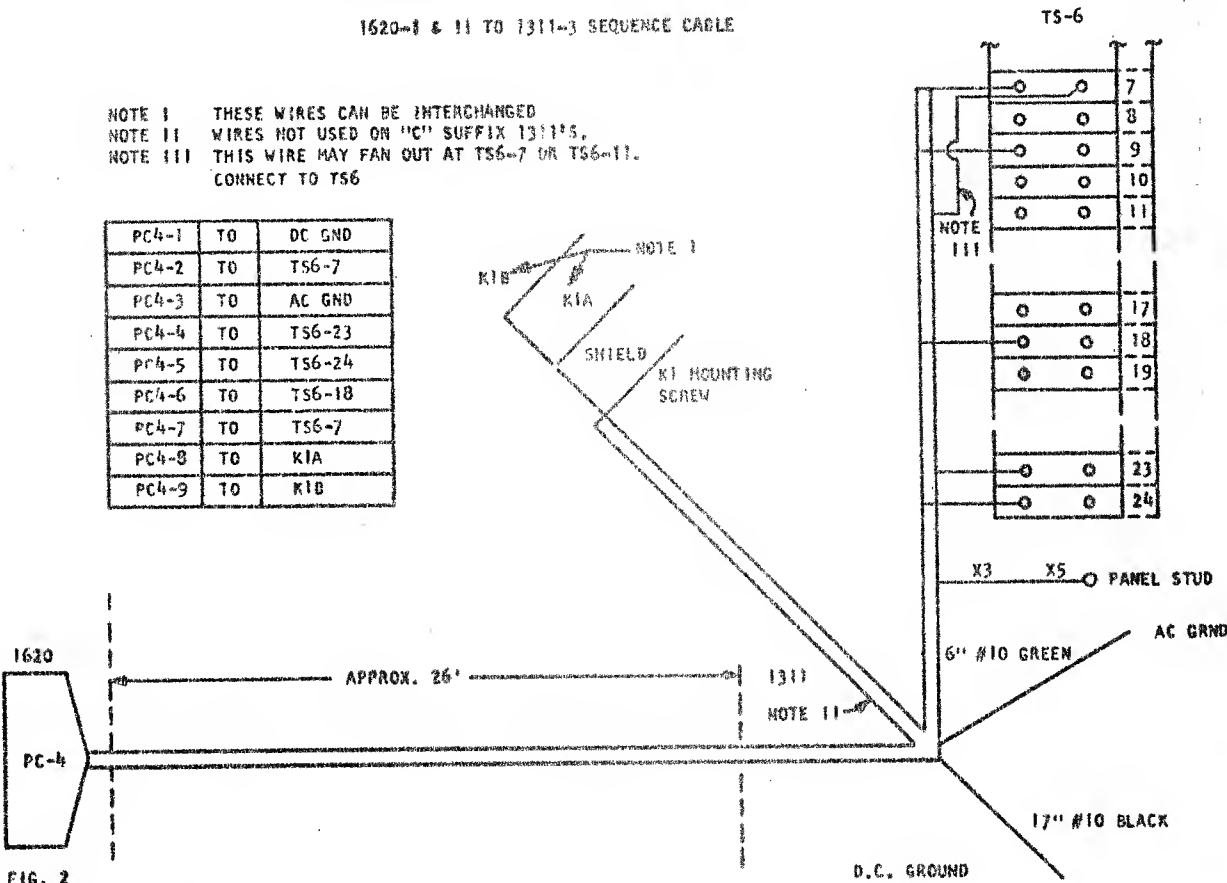
NOTE: THE 1311 SUFFIX CAN BE FOUND AT THE TOP OF THE FIRST PAGE OF THE LOGICS. BEFORE INSTALLING ANY CABLES, CHECK R/W GROUND BUS (A06J OF B GATE) TO FRAME GROUND. READING SHOULD BE OPEN CIRCUIT OR HIGHER THAN 5 MEGOHM. ANY LOWER READING INDICATES A FRAME GROUND ON THE MACHINE BASE PLATE OR THE R/W GROUND BUS.

NOTE: TO PREVENT INTERACTION BETWEEN CABLES, CABLES THAT DO NOT TIE INTO THE 1311 FILES SHOULD BE LOCATED AT LEAST ONE FOOT AWAY FROM THE PROCESSOR TO THE FILE AND INTERFILE CABLING. ORIENT CABLES AS SHOWN IN FIGURE 3. FOR 1620-11 CABLES, REFER TO INSTALLATION INSTRUCTIONS IN 1620 11 LOGIC.

INSTALL SEQUENCE CABLE BETWEEN PROCESSOR AND MOD 3 (USE CABLE DRAWING SHOWN IN FIGURE 2 AND SECTION 07, XX IN THE REFERENCE SECTION OF 1LD.) ON B SUFFIX, THE LONGEST LEG OF THIS CABLE IS ROUTED THROUGH HOLE IN RIGHT END OF SEQUENCE BOX, THROUGH CABLE CLAMP TO K1 CONTACTOR. THE TWO WIRES TO K1 ARE NOT POLARIZED SINCE THIS IS AN AC CONTACTOR. ON C SUFFIX, K1 CONTACTOR WAS REMOVED AND LEADS ARE UNUSED AND TAPED IN CABLE.

INSTALL THE AC POWER CABLE BETWEEN THE 1311 MOD 3 AND THE 1620. ON "B" SUFFIX 1311'S CONNECT THE AC LEADS TO THE CIRCUIT BREAKER IN THE SEQUENCE BOX. CONNECT THE GROUND STRAP AND THE GREEN LEAD TO A SEQUENCE BOX MOUNTING STUD. (FRAME GROUND). ON "C" SUFFIX 1311'S CONNECT AC LINES TO THE DISCONNECT SWITCH AND GROUND STRAP AND GREEN WIRE TO THE GROUND STUD NEXT TO INLET CABLE CLAMP. REFER TO LOGIC PAGE 05.40.01.1.

1620-1 & 11 TO 1311-3 SEQUENCE CABLE



C. SATELLITE INSTALLATION

If "D" suffix satellite is to be attached to a "B" satellite master, B/K 2165415, "Install Satellite Power Compatibility" must be installed. To determine whether this FOM is installed, proceed as follows:

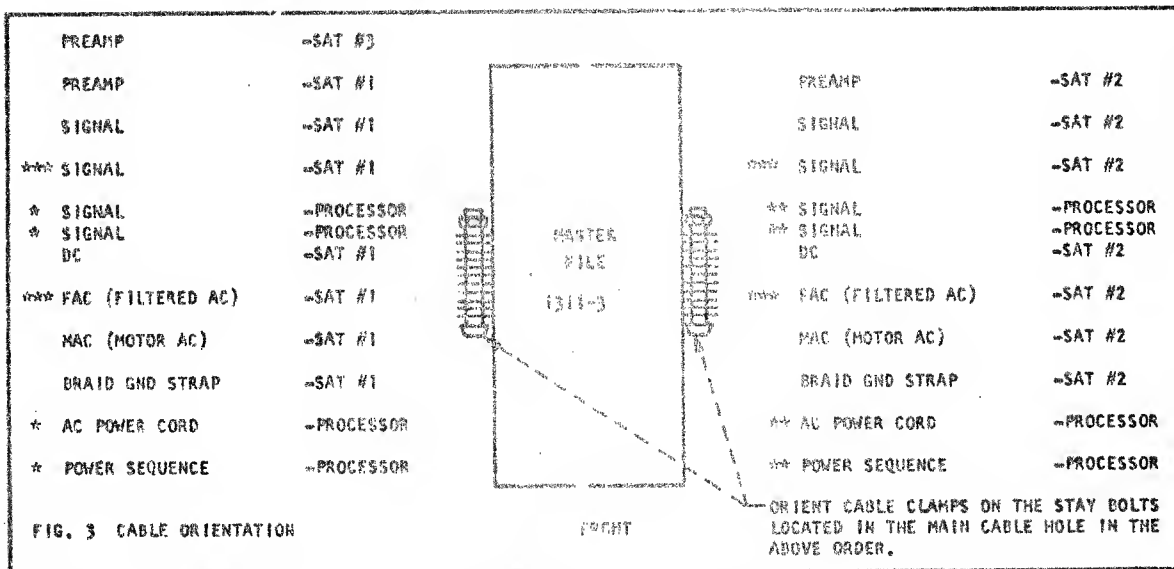
Remove all power from the system, this includes removal of mainline AC Power Plug from the wall, then check for continuity between K1-U1 and TS3-1. If there is continuity, this FOM is installed. If not, you must order and install the aforementioned field bill of material. For temporary expediency follow the instructions below. Use #14 wire or larger.

1. All system power must be off.
2. Remove leads at K1 U1 & U3 connecting to TS3-1 & 2. Disconnect both ends and tape back.
3. Install jumpers from K2 U1 to TS3-1 and K2 U2 to TS3-2.
4. The single AC plug from the D suffix satellite plugs into the MAC receptacle.
5. Modify logic page 05.40.01.1 at DA 303000 or lower to show the above change.

BEFORE INSTALLING ANY CABLES, CHECK R/W GROUND BUS (AG6 OF A GATE) TO FRAME GROUND. READING SHOULD BE HIGHER THAN 5 MEGOHM AFTER NEEDLE OF METER HAS STABILIZED. ANY LOWER READING INDICATES A FRAME GROUND ON THE MACHINE BASE PLATE OR THE R/W GROUND BUS.

THE NUMBER OF CABLE CONNECTIONS, ETC., DEPENDS ON THE NUMBER OF SATELLITES ACTUALLY BEING INSTALLED. IF THE INSTALLING CE ELECTS TO CABLE AND TEST THE FILES ONE AT A TIME, HE MUST OBSERVE THE RULES FOR CARD PLUGGING AND MOTOR SEQUENCE LOOP JUMPERS AS PER THE FILE CONFIGURATION HE IS TESTING.

1. UNPACK AND UNROLL CABLES.
2. UNROLL GROUND STRAP AND ROUTE OUT OF SIDE HOLE IN THE SEQUENCE BOX AND THEN OUT THROUGH THE MAIN CABLE ACCESS HOLE. GROUND STRAP IS SHIPPED COILED UP IN SEQUENCE BOX.
3. ORIENT CABLES AND GROUND STRAP AS SHOWN IN FIG. 3 AND SECTION 07.XX UNDER "CABLE CONNECTIONS."



* THESE CABLES PRESENT ONLY IF PROCESSOR IS ORIENTED TO LEFT OF FILES.

** THESE CABLES PRESENT ONLY IF PROCESSOR IS ORIENTED TO RIGHT OF FILES.

*** NOT PRESENT FROM "D" SUFFIX SATELLITES.

NOTE: IF RAISED FLOOR IS USED, * AND ** CABLES MAY BE ORIENTED AS REQUIRED.

4. ROUTE COAX CABLES UNDER ANY ADJACENT SATELLITE AND THEN UNDER THE MASTER FILE AND UP THROUGH MASTER FILE MAIN CABLE ACCESS HOLE.

5. FEED COAX CABLE UP THE HINGE END OF B GATE AND UNDER THE DISCUIT CONNECTOR MOUNTING FOR A ROW. DO NOT SECURE CONNECTOR BRACKET UNTIL ALL SATELLITE COAX CABLES HAVE BEEN INSTALLED. THE NYLON CLAMP UNDER THE DISCUIT CONNECTOR CAN BE MOUNTED TWO WAYS, ONE WAY FOR RIBBON OR SMALL CABLES AND ANOTHER WAY, BY REVERSING IT, FOR LARGER CABLES. MOUNT THIS CLAMP FOR THE BEST STRAIN RELIEF-DEPENDING ON HOW MANY SAT. CABLES ARE INSTALLED.

FEED THE COAX CABLE THROUGH THE CABLE CLAMP AT THE TOP OF THE DC DISTRIBUTION BUS. CHECK THAT CABLES DO NOT PRESS AGAINST PINS AT POSITION A01, AND THAT MACHINE COVER DOES NOT PRESS AGAINST SATELLITE COAX CABLES WHEN GATE IS CLOSED AND COVERS REPLACED.

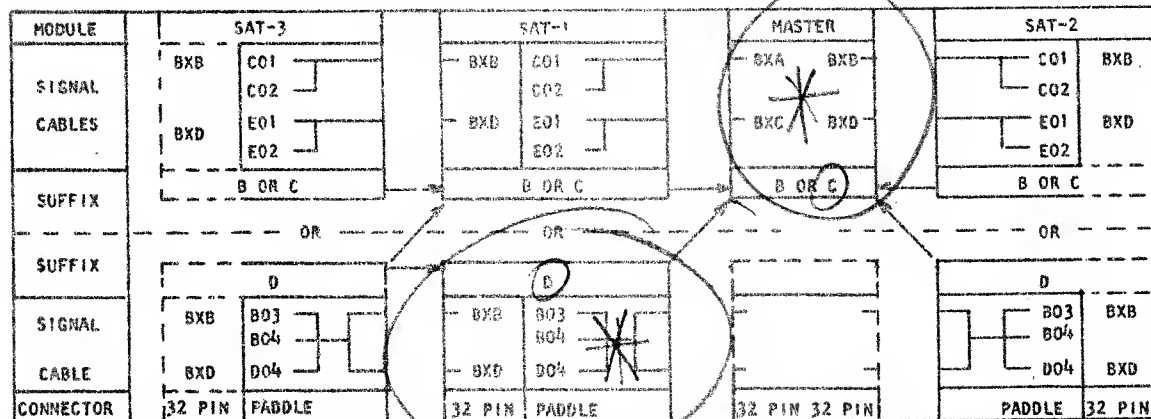
6. CONNECT SATELLITE COAX TERMINALS AS FOLLOWS ON GATE B:

	SHIELD	COAX COMMONS	ONE WIRE OF PRE AMP SIGNAL	ONE WIRE OF PRE AMP SIGNAL
SAT. #=1	R/W GND. BLOCK	A10J	A10A	A10D
SAT. #=2	R/W GND. BLOCK	A11J	A10H	A10E
SAT. #=3	R/W GND. BLOCK	A11J	A10Q	A10F

NOTE: ANY R/W GROUND, PIN J OF "A" ROW -B THROUGH 15 MAY BE USED IF 2 SLIP-ONS DO NOT FIT ON ANY ONE COAX COMMON PIN. NOW SECURE BRACKET OVER COAX CABLES.

7. SELECT PROPER SIGNAL CABLE FOR EACH SATELLITE (SEE STEP 8.). ROUTE SIGNAL CABLE UNDER MACHINE AND UP THROUGH MAIN CABLE ACCESS HOLE OF ADJACENT FILE. SAT. #1 AND SAT. #2 WILL GO TO THE MASTER; SAT. #3 TO SAT. #1. ADJUST AND FASTEN CABLE CLAMPS AFTER INSTALLING CONNECTORS.

8. CONNECT SATELLITE SIGNAL CABLES AS FOLLOWS:



Note that the paddle side of the B & C suffix satellites require 2 signal cables while the paddle side of the D suffix satellite uses 1 cable. Also, whenever a B or C suffix satellite is connected to a D suffix satellite, the B or C must be placed nearest the Master in order to satisfy the satellite power connection requirements.

9. ROUTE DC CABLES UNDER MACHINE AND UP THROUGH MAIN CABLE ACCESS HOLE OF ADJACENT FILE. CONNECT AS FOLLOWS:

FROM	TO
SAT. #=1	MASTER DC-2
SAT. #=2	MASTER DC-1
SAT. #=3	SAT. # 1 DC

CONNECT GROUND LEADS OF CABLES TO RESPECTIVE GROUND BUS. INSTALL CABLE CLAMPS.

10. ROUTE AC CABLES UNDER MACHINE AND UP THROUGH POWER CABLE ACCESS HOLE UNDER SEQUENCE BOX OF ADJACENT FILE. CONNECT AS FOLLOWS: (NOTE: THE D SUFFIX SATELLITE HAS ONLY ONE POWER CABLE; IT SHOULD BE PLUGGED INTO THE MAC RECEPTACLE.)

FROM	TO
SAT. #=1	MASTER MAC-2 FAC-2
SAT. #=2	MASTER MAC-1, FAC-1
SAT. #=3	SAT. # 1 MAC, FAC

11. ROUTE BRAIDED GROUND STRAP FROM SEQUENCE PANEL UNDER MACHINE AND UP THROUGH MAIN CABLE ACCESS HOLE AND THEN THROUGH THE HOLE IN THE SIDE OF THE SEQUENCE BOX OF THE ADJACENT FILE. CONNECT STRAP JUST INSIDE SEQUENCE BOX WHERE THE FOUR TAPPED HOLES WITH SCREWS ARE PROVIDED:

FROM	TO
SAT. #=1	MASTER
SAT. #=2	MASTER
SAT. #=3	SAT. # 1

D. SMS CARD INSTALLATION

SPECIAL FEATURES REQUIRE ADDITION OR REMOVAL OF CARDS. THE REQUIREMENT FOR EACH FEATURE ARE INDICATED BY CODE LETTERS OPPOSITE THE CARD TYPE ON THE UNIT PLUGGING CHART. SEE 05.00.75.1 (A-GATE) AND 05.00.80.1 (B-GATE). THE CODE DESIGNATIONS ARE SHOWN ON THE FOLLOWING CHART.

MODS USING 2 3	FEATURE CODE	D/A CODE	FEATURE
X	ASC		ANY SEEK COMPLETE
X X	DIA		DIRECT ACCESS (DIRECT SEEK)
X	DSOV		DIRECT SEEK OVERLAP
X	MM		MULTI MODULE
X X	NDIA		NON DIRECT ACCESS
X	NMI		NON ADDITIONAL MEMORY (1623)
X	SCI		SEEK INTERRUPT
X	SOV		SEEK OVERLAP

THE INSTALLATION OF SATELLITE FILES DOES NOT REQUIRE EXTRA CARDS TO BE PLUGGED INTO THE 1620 PROCESSOR.

MASTER FILES

IF THE SYSTEM IS A 1620 - 1 WITH ADDITIONAL MEMORY, THE NMI (NOT ADDITIONAL MEMORY) FEATURE CARDS IN THE 1311 MOD 3 SHOULD BE REMOVED. IF THE SYSTEM IS A 1620 - 11 WITH OR WITHOUT ADDITIONAL MEMORY OR 1620 - 1 WITHOUT ADDITIONAL MEMORY, THE NMI CARDS SHOULD BE INSTALLED. THESE CARDS MUST BE CORRECTLY INSTALLED IN ORDER TO TERMINATE THE MAR LINES.

MULTIPLE FILE SYSTEMS MUST HAVE EXTRA CARDS PLUGGED IN THE MASTER FILE. THESE CARDS ARE INSTALLED WITH ONE OR MORE SATELLITES. REFER TO 1311-3 UNIT PLUGGING CHART. ALL CARDS CODED MM (MULTI MODULE) MUST BE INSTALLED.

SATELLITE FILES

REQUIRED CARDS AND JUMPER WIRES AS INDICATED BELOW, ARE SUPPLIED WITH FACTORY SHIPPED MASTER FILES IN AN ENVELOPE LOCATED BETWEEN THE SEQUENCE PANEL AND THE 1311 SIDE PANEL. FOR FIELD TRANSFERRED MACHINES, PARTS MUST BE OBTAINED LOCALLY OR ORDERED.

SATELLITE FILES WITH MODEL 3 MASTER.

1. SINGLE SATELLITE SYSTEM. A SINGLE SATELLITE SYSTEM MUST HAVE THE FOLLOWING CARDS PLUGGED IN THE SATELLITE: NOTE: SUFFIX LEVEL IS SHOWN AT TOP OF FIRST PAGE OF LOGIC BOOK.

CARD TYPE	POSITION
AZE	E04 ("B" & "C" SUFFIX MOD 2) OR E06 ("D" SUFFIX MOD. 2)
AZE	E05 ("B" & "C" SUFFIX MOD 2) OR E07 ("D" SUFFIX MOD. 2)
AZF	E06 ("B" & "C" SUFFIX MOD 2) OR E08 ("D" SUFFIX MOD. 2)
AZF	E07 ("B" & "C" SUFFIX MOD 2) OR E09 ("D" SUFFIX MOD. 2)

2. MORE THAN ONE SATELLITE SYSTEM. A SYSTEM WITH MORE THAN ONE SATELLITE MUST HAVE THE FOLLOWING CARDS INSTALLED IN THE HIGHEST ODD-NUMBERED SATELLITE ONLY:

CARD TYPE	POSITION
AZE	E04 ("B" & "C" SUFFIX MOD 2) OR E06 ("D" SUFFIX MOD 2)
AZE	E05 ("B" & "C" SUFFIX MOD 2) OR E07 ("D" SUFFIX MOD 2)

ALL OTHER "B" OR "C" SUFFIX SATELLITES MUST NOT HAVE CARDS INSTALLED IN E04 OR E05; AND ALL OTHER "D" SUFFIX SATELLITES MUST NOT HAVE CARDS INSTALLED IN E06 OR E07.

THE FOLLOWING CARDS MUST BE INSTALLED IN SATELLITE #2 ONLY:

CARD TYPE	POSITION
AZF	E06 ('B' & 'C' SUFFIX MOD 2) OR E08 ('D' SUFFIX MOD 2)
AZF	E07 ('B' & 'C' SUFFIX MOD 2) OR E09 ('D' SUFFIX MOD 2)

ALL OTHER 'B' SUFFIX SATELLITES MUST NOT HAVE CARDS INSTALLED IN E06 OR E07; ALL OTHER 'C' SUFFIX SATELLITES MUST NOT HAVE CARDS INSTALLED IN E06 OR E07; AND ALL OTHER 'D' SUFFIX SATELLITES MUST NOT HAVE CARDS INSTALLED IN E08 OR E09.

SATELLITE FILES - MOTOR SEQUENCE LOOP.

TWO JUMPERS, P/N 535869, MUST BE INSTALLED ON THE HIGHEST ODD-NUMBERED SATELLITE ONLY AS FOLLOWS:

(B & C SUFFIX)		(D SUFFIX)	
FROM	TO	FROM	TO
TS5-7	TS5-19	TS6-7	TS6-9
TS5-8	TS5-20	TS6-8	TS6-10

THESE JUMPERS MUST NOT BE INSTALLED ON ANY OTHER SATELLITE.

SATELLITE FILES - PREAMP JUMPER.

WITH MOD 3 MASTER, THERE MUST NOT BE A PREAMP JUMPER BETWEEN 02B1 A06A AND B ON ANY SATELLITE.

E. MECHANICAL CHECKS.

1. RAISE MACHINE ON GLIDER SUFFICIENTLY SO THAT CASTERS CAN BE REMOVED, THEN LOWER SO MACHINE IS LEVEL AND 1-1/8" OFF THE FLOOR.
2. WITH TOP COVER REMOVED, CHECK FOR OIL LEAKS.
3. CHECK ARM ASSEMBLIES TO SEE THAT:
 - a. TORSION BAR SEATING IS CORRECT.
 - b. ARMS ARE SEATED AGAINST THE BACK STOP SCREWS.
 - c. ARM ASSEMBLY CLAMPS ARE TIGHT.

WARNING: DO NOT PUSH TOO HARD. CARRIAGE RACK CAN BE DISENGAGED FROM PINION GEAR ON EARLY MACHINES. FOR REALIGNMENT SEE C.E.R.M.

- d. HEAD CABLE PLUGS ARE SEATED.
4. INSPECT PHOTOCELL ASSEMBLIES FOR:
 - a. LOOSE MOUNTING SCREWS.
 - b. LOOSE TERMINALS.
 - c. LOOSE OR UNSEATED LAMPS.
 5. CHECK SOLENOID TERMINAL BLOCKS FOR LOOSE SL -ON TERMINALS OR SHORTS.
 6. CHECK MOTOR DRIVE BELT FOR PROPER INSTALLATION. (SEE C.E.R.M.)
 7. CHECK COMPARE DISABLE SWITCH IN MASTER FOR PROPER ADJUSTMENT SO IT WILL TURN OFF AUTOMATICALLY WHEN B-GATE IS CLOSED.
 8. CHECK FOR PROPER SATELLITE 'ID' DOT ON INDICATOR AT THE LEFT END OF OPERATOR PANEL ON EACH SATELLITE UNIT BEING INSTALLED. SEE NOTE 5 ON FIGURE 1.

F. FILE POWER CHECK

TRANSFORMER PRIMARY CHECK

MACHINES ARE SHIPPED WITH TRANSFORMER PRIMARIES WIRED ACCORDING TO ORDER. IF CUSTOMER'S SUPPLY IS DIFFERENT, WIRES TO PRIMARY TRANSFORMER TAPS MUST BE MOVED AS INDICATED IN FIGURE 4. REMOVE THE 200V VOLTAGE LABELS IF THE TAPS ARE CHANGED TO 230 VOLTS.

FOR 50 CYCLE MOD III, THE INPUT VOLTAGE ON THE SUPPLIES MAY BE 195, 220 OR 235 V AC, AND TRANSFORMER TAPS MUST BE MOVED AS IN FIGURE 5.

VOLTAGE CHECK BE SURE THE MAIN POWER SWITCH (ON THE WALL) IS OFF. PLUG THE FILE POWER CORD INTO THE LINE FILTER BOX LOCATED IN THE 1620. TURN MAIN POWER SWITCH ON. TURN SYSTEM POWER ON. CHECK THE FOLLOWING VOLTAGES AT THE ELECTRONIC GATE ON THE MASTER FILE AND ON EACH SATELLITE:

MOD. 2. REFER TO SATELLITE SYSTEM DIAGRAM C2.02.25.1.

-36V (R/W)
-12V
-36V
+12V
-6V
DC GROUND

MOD. 3 REFER TO SYSTEM DIAGRAMS 05.40.10.1 AND 05.40.11.1

A GATE:	B GATE:
-12V	-36V (R/W)
+12V M	-12V
-6V	-36V
DC GROUND	+12 V M
	-6V
	+12V
	DC GROUND

BLOWER CHECK

CHECK BLOWERS IN EACH GATE; CHECK POWER SUPPLY FANS (MOD 3) FOR PROPER OPERATION.

PHOTOCELL LAMP CHECK

CHECK THAT PHOTOCELL LAMPS ARE ON AND THAT LIGHT SPOT IS PROPERLY ORIENTED. PHOTOCELL SLIT MUST BE CENTERED IN SPOT.

BE SURE THAT ALL START/STOP SWITCHES ARE OFF. TURN OFF SYSTEM POWER USING DC POWER SWITCH.

G. HEAD-DISK CHECK (POWER OFF).

WARNING: DURING THESE CHECKS DO NOT ALLOW HEADS TO LOAD ON DISKS.

1. CLEAN ALL HEADS, SEE C.E. REF. MAN.
2. INSPECT DISK PACK FOR POSSIBLE SHIPPING DAMAGE AS DESCRIBED IN C. E. REF. MAN.
3. CLEAN DISK PACKS, SEE C. E. REF. MAN. TURN POWER ON WHILE INSTALLING PACKS SO BRAKE WILL OPERATE. TURN POWER OFF.
4. MANUALLY TRIP MECHANICAL HEAD LOADING LATCH UNDER FORWARD END OF CARRIAGE RACK TO AVOID LOADING HEADS, AND MANUALLY MOVE CARRIAGE FORWARD INTO DISK PACK.

WARNING: DO NOT ALLOW HEADS TO LOAD ON DISKS.

- CHECK CLOSELY FOR INTERFERENCE---ANY RUBBING OF HEADS OR HEAD CABLES, BINDS, ETC.,---RUN CARRIAGE ALL THE WAY TO POSITIVE STOP.
- RESTORE CARRIAGE BACK TO MECHANICAL HOME.

5. CHECK FOR PROPER SECTOR BLOCK TO SECTOR DISK ADJUSTMENT AND CLEARANCE.

6. REPEAT STEP 4 AND STEP 5 ON ALL FILES.

H. FILE MOTOR AND HEAD LOADING CHECK.

1. REMOVE EACH DISK PACK IN TURN AND PERFORM THE FOLLOWING STEPS ON ALL FILES.

- VACUUM ENTIRE BASE PLATE AREA, VISIBLE PORTION OF MODULE TOP, AND CLEAN INSIDE SHROUD, (SEE C.E.R.M.)
- REPLACE TOP COVER ASSEMBLY AFTER CHECKING THAT IT IS CLEAN.

2. REPLACE ALL DISK PACKS (DATA PACKS).

NOTE: ALL FILE START/STOP SWITCHES SHOULD BE OFF.

3. TURN SYSTEM POWER ON USING DC POWER SWITCH.

4. DEPRESS MASTER START/STOP SWITCH.

- CHECK THAT MOTOR COMES ON.
- CHECK THAT AUTOMATIC HEAD INSERTION AND HEAD LOADING OCCURS WHEN THE DISK PACK GETS UP TO SPEED (AFTER PROPER DELAY). WHEN HEADS ARE LOADED, USE FLASHLIGHT TO CHECK THAT HEAD CABLES PROPERLY CLEAR DISKS.
- CHECK THAT ACCESS DETENTS AT TRACK ZERO.
- CHECK THAT READY LIGHT IS ON.
- CHECK FOR OIL LEAKS.

5. ELECTRICAL HEADS UNLOAD CHECK.

CAUTION: IN THE FOLLOWING PROCEDURE KEEP FINGERS OUT OF AREA BETWEEN CARRIAGE AND HYDRAULIC UNIT AND BETWEEN CARRIAGE AND CARRIAGE HOUSING.

- LIFT LEFT SIDE OF TOP COVER.
- STANDING IN FRONT OF MACHINE, WITH THE LEFT HAND RESTRAIN THE CARRIAGE FROM MOVING IN (CARRIAGE WON'T MOVE UNTIL STEP C BELOW) BY HOLDING UPPER REAR SECTION OF CARRIAGE ASSEMBLY.
- WITH RIGHT HAND PULL THE DETENT AND ALLOW CARRIAGE TO MOVE SLOWLY IN (MOTOR IS STILL ON).
- ALLOW DETENT TO SET ANYWHERE BETWEEN TRACK 50 AND 99.
- CHECK TO SEE THAT THE HEADS ARE STILL LOADED.
- FIRMLY RESTRAIN THE CARRIAGE ASSEMBLY FROM MOVING DURING THE NEXT STEP, UNLESS OTHERWISE INDICATED.

WARNING: IN THE FOLLOWING STEP DO NOT ALLOW THE DISKS TO APPRECIABLY SLOW DOWN.

- WHILE WATCHING THE HEADS, HIT THE START/STOP KEY. IF THE HEADS DO NOT IMMEDIATELY UNLOAD, HIT THE START/STOP KEY AGAIN TO RETURN TO NORMAL DISK SPEED. IF THE HEADS DO UNLOAD, ALLOW THE CARRIAGE TO RETRACT TO HOME POSITION WHERE IT WILL DETENT.
- IF THE HEADS DID NOT UNLOAD ON THE STEP ABOVE, PULL THE ARMATURE AWAY FROM THE HEAD LATCH MAGNET. THE HEADS WILL UNLOAD.
- DETERMINE WHY THE ELECTRICAL HEADS UNLOAD CIRCUITS DO NOT WORK BEFORE PROCEEDING.

6. DO THE HEAD UNLOAD KNOCK-OFF CHECK. FOLLOW THIS PROCEDURE:

- WITH THE LINKAGE IN UNLOADED CONDITION AND WITH THE LATCH HELD AGAINST THE LINK (SEE C.E.R.M.), CHECK THAT THE KNOCK-OFF PLUNGER CONTACTS THE ROLLER ARM IN THE RANGE OF CARRIAGE TRAVEL BETWEEN MINUS TRACK 5 AND MINUS TRACK 7.5.
- ADJUST BY FORMING THE UPPER LEG OF THE ARMATURE OR BY SHIFTING THE POSITION OF THE ROLLER ARM (ELONGATED HOLES). IF THE ROLLER ARM POSITION IS CHANGED, CHECK THE .005" - .015" CLEARANCE BETWEEN THE ROLLER ARM AND THE MOVABLE CARRIAGE (SEE C.E.R.M.)

7. CLOSE TOP COVERS.

8. TURN START/STOP SWITCH ON.

9. REPEAT STEPS 5 THROUGH 9 FOR EACH SATELLITE FILE.

10. WITH ALL FILE MOTORS ON, TURN SYSTEM POWER OFF USING DC POWER SWITCH. ALL MOTORS SHOULD TURN OFF, ALL HEADS SHOULD UNLOAD, AND ALL CARRIAGES SHOULD RETRACT.

I. POWER ON MOTOR SEQUENCE CHECK.

NOTE: LET ALL FILES COME TO A STOP AND BE SURE THAT THE MOTOR SEQUENCE LOOP WIRING IS INSTALLED IN THE HIGHEST ODD-NUMBERED SATELLITE. (SEE MOTOR SEQUENCE LOOP SECTIONS OF INSTALLATION FOR SATELLITE #1 AND SATELLITE #3.) CHECK THAT SATELLITE #2 DOES NOT HAVE MOTOR SEQUENCE WIRING (SEE C2.06.03.3).

1. TURN ON SYSTEM POWER USING DC POWER SWITCH.

2. MASTER FILE MOTOR SHOULD COME ON IMMEDIATELY.

3. AT THIS POINT THE SEQUENCE IN WHICH THE SATELLITE FILE MOTORS TURN ON DEPENDS UPON THE NUMBER OF SATELLITES IN THE SYSTEM. THE TABLE BELOW INDICATES THE SEQUENCE PATTERN DEPENDS UPON THE NUMBER OF SATELLITES.

SATELLITE MOTOR SEQUENCING

2 SATELLITE SYSTEM	3 SATELLITE SYSTEM
SATELLITE #1 SATELLITE #2	SATELLITE #1 SATELLITE #3 SATELLITE #2

NOTE: NO TWO FILE MOTORS SHOULD COME ON AT THE SAME TIME.

J. HEAD ALIGNMENT

- REMOVE DISK PACK FROM MASTER FILE.
- INSTALL CE DISK PACK ON MASTER FILE AND CHECK FOR PROPER HEAD ALIGNMENT (SEE C.E. REF. MANUAL FOR PROCEDURES).
- REPEAT STEPS 1 AND 2 FOR ALL SATELLITES.
- REMOVE CE DISK PACK FROM LAST FILE CHECKED.
- INSTALL DATA DISK PACKS ON ALL FILES.

K. GENERAL CHECKS

Run functional tests to check operation of files and systems. Be sure to run applicable portion of system meter verification test to check meter operation. If the system is not metered, Feature B/M 2134174 must be installed to activate the 1311 meter(s); then verify correct meter operation (use specs from above test).

MODEL	POWER SUPPLY UNIT	TRANSFORMER PART NO.	LOCATION	SYSTEM DIAGRAM	208 V CONNECTIONS	230 V CONNECTIONS
1311-2 B&C SUFFIX	-36 V 8% 2.5A	801640	02B1A13	C2.12.02.1	JUMPER TAPS 1-4	JUMPER TAPS 1-5
	METER PWR PAC	740473	FILE FLOOR	C2.32.20.1	TAPS 1&4	TAPS 1&5
1311-3 D SUFFIX	-36VDC Supply	(Refer to logic page)		C2.12.01.1		
	FERRO RES 133V	208269	TOP RIGHT SMS POWER SUPPLY BOX	05.40.01.1	AC INPUT ON TERMINALS 1&4	AC INPUT ON TERMINALS 1&5
	24V TRANSFORMER	2128759	BACK SIDE SMS POWER SUPPLY BOX	05.40.01.1	AC INPUT ON TERMINALS 1&2	AC INPUT ON TERMINALS 1&3
	-36 V 2%	801580	D GATE LOC B2	05.40.05.1	JUMPER TAPS 1-4	JUMPER TAPS 1-5
	-36 V 8%	801640	D GATE LOC E2	05.40.09.1	JUMPER TAPS 1-4	JUMPER TAPS 1-5
	+12 V 2%	801577	D GATE LOC C14	05.40.06.1	JUMPER TAPS 1-4	JUMPER TAPS 1-5
	METER PWR PAC	740473	FILE FLOOR	C2.32.30.1	TAPS 1&4	TAPS 1&5

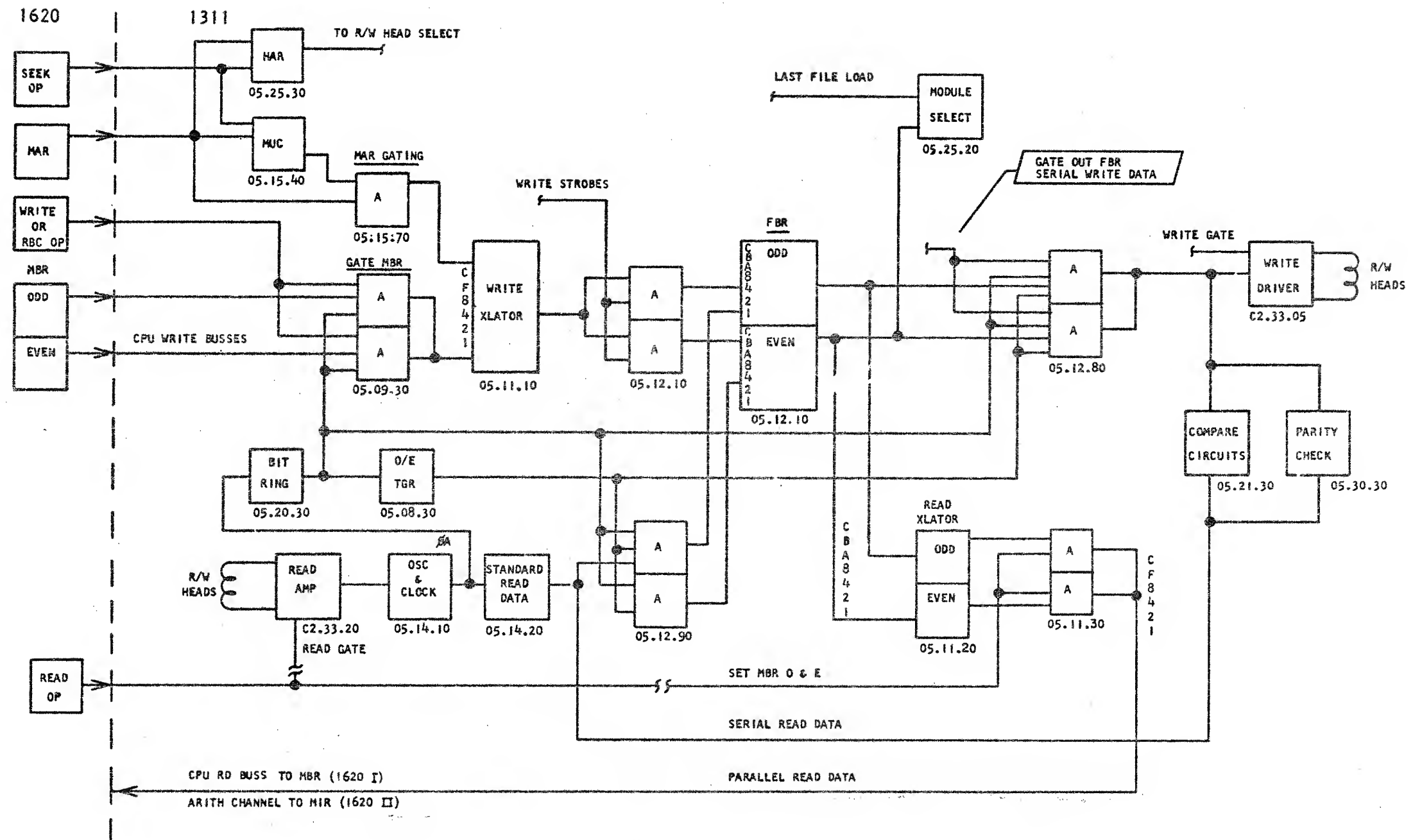
FIGURE 4. TRANSFORMER CONNECTIONS - 60 CYCLE

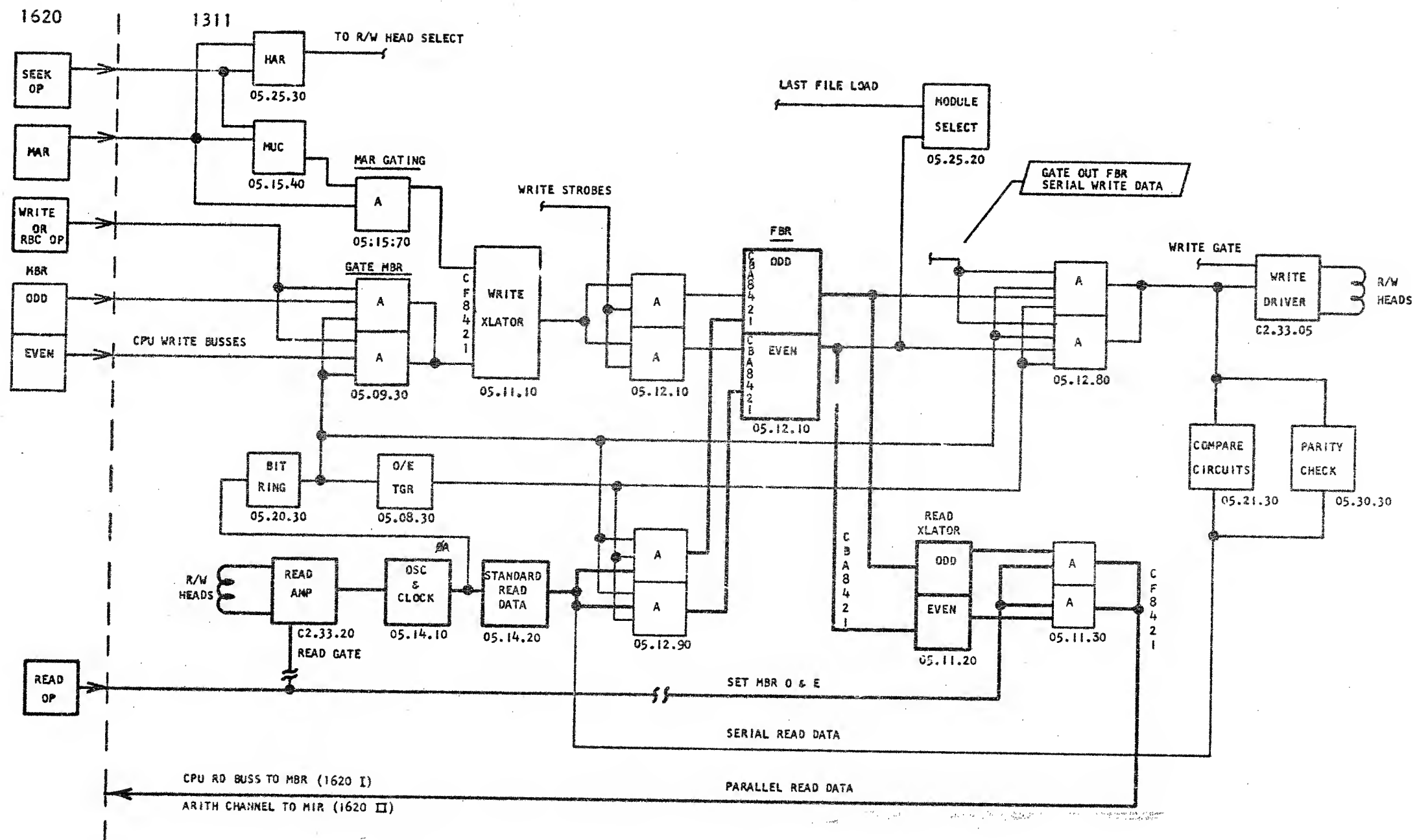
MODEL	POWER SUPPLY	TRANS P/N	LOGIC	AC	195V	220V	235V
1311-2 B&C SUFFIX	VDC -36 (8%)	5240451	C2.12.02.1	02B1A13	JUMPER TAPS 1-4	JUMPER TAPS 1-5	JUMPER TAPS 2-3P
	METER PWR PAC	740561	C2.32.30.1	FILE FLOOR	TAPS 1&3	TAPS 1&4	TAPS 1&5
1311-3 D SUFFIX	-36 VDC Supply	(Refer to logic page)					
	VAC 133 FERRO	4117546	05.40.01.1	TOP RIGHT SMS TUB	AC PRI.ON TAPS 1&2	AC PRI.ON TAPS 1&3	AC PRI.ON TAPS 1&4
	VAC 24V XFMR	2132440	05.40.01.1	BACK OF SMS TUB	AC PRI.ON TAPS 1&2	AC PRI.ON TAPS 1&3	AC PRI.ON TAPS 1&4
	VDC -36 (2%)	801631	05.40.05.1	B-2 D GATE	JUMPER TAPS 1-4	JUMPER TAPS 1-5	JUMPER TAPS 2-3P
	VDC -36 (8%)	5240451	05.40.09.1	E-2 D GATE	JUMPER TAPS 1-4	JUMPER TAPS 1-5	JUMPER TAPS 2-3P
	VDC +12 (2%)	801629	05.40.06.1	C14 D GATE	JUMPER TAPS 1-4	JUMPER TAPS 1-5	JUMPER TAPS 2-3P
	METER PWR PAC	740561	C2.32.30.1	FILE FLOOR	TAPS 1&3	TAPS 1&4	TAPS 1&5

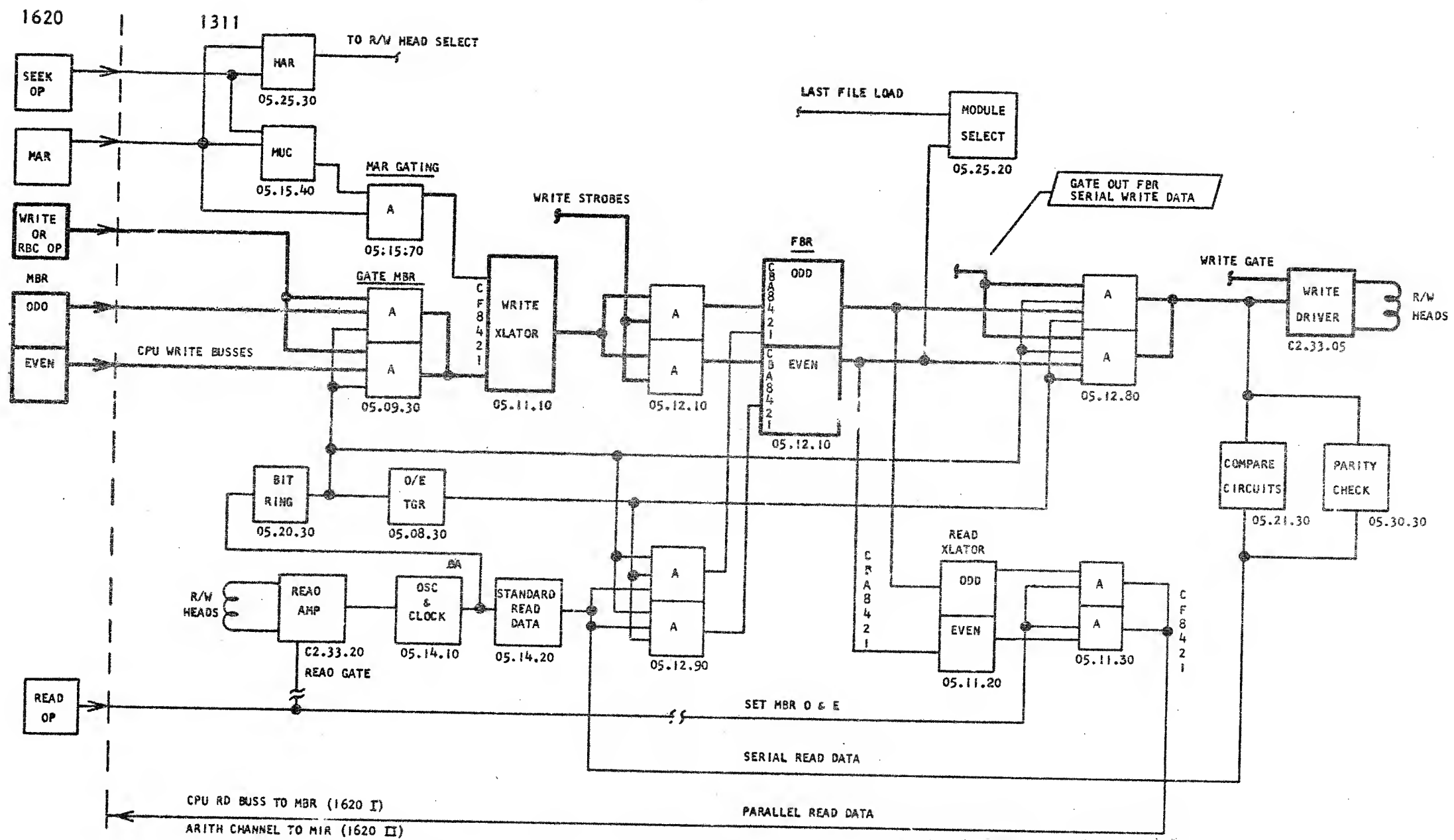
FIGURE 5. TRANSFORMER CONNECTIONS - 50 CYCLE

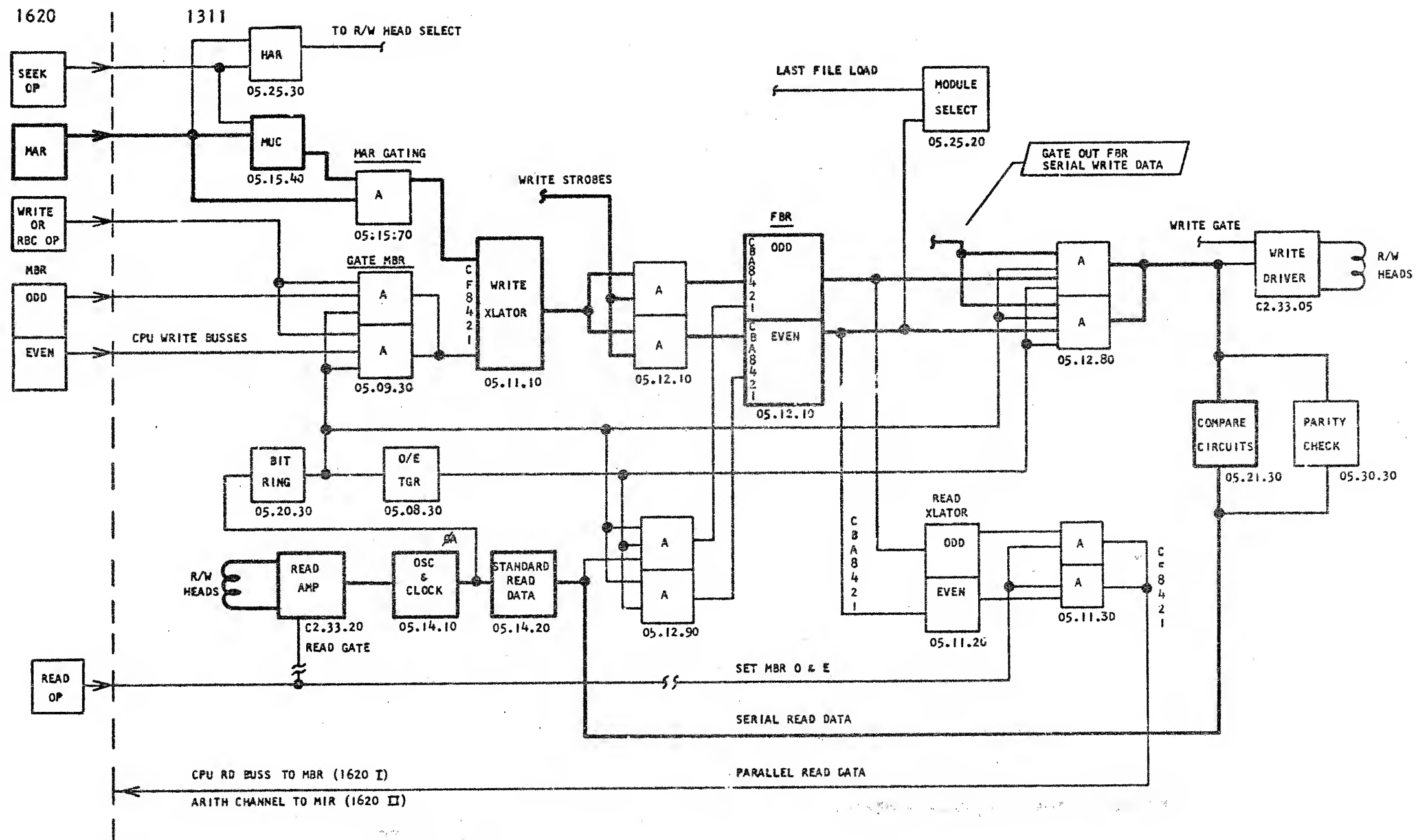
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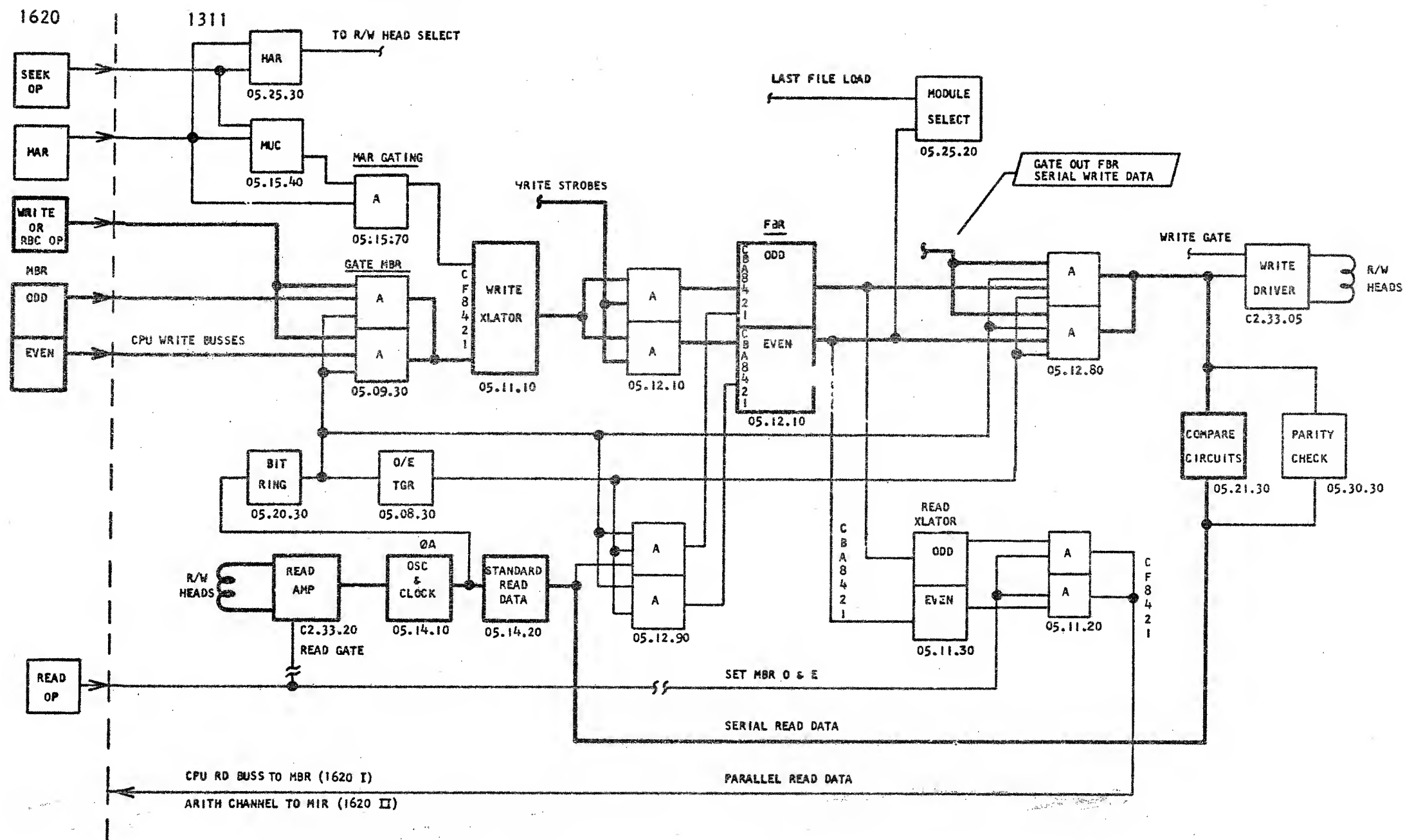
GENERAL DATA FLOW	02.01
READ DATA FLOW	02.02
WRITE DATA FLOW	02.03
ADDRESS COMPARE DATA FLOW	02.04
READ BACK CHECK DATA FLOW	02.05
SEEK DATA FLOW	02.06

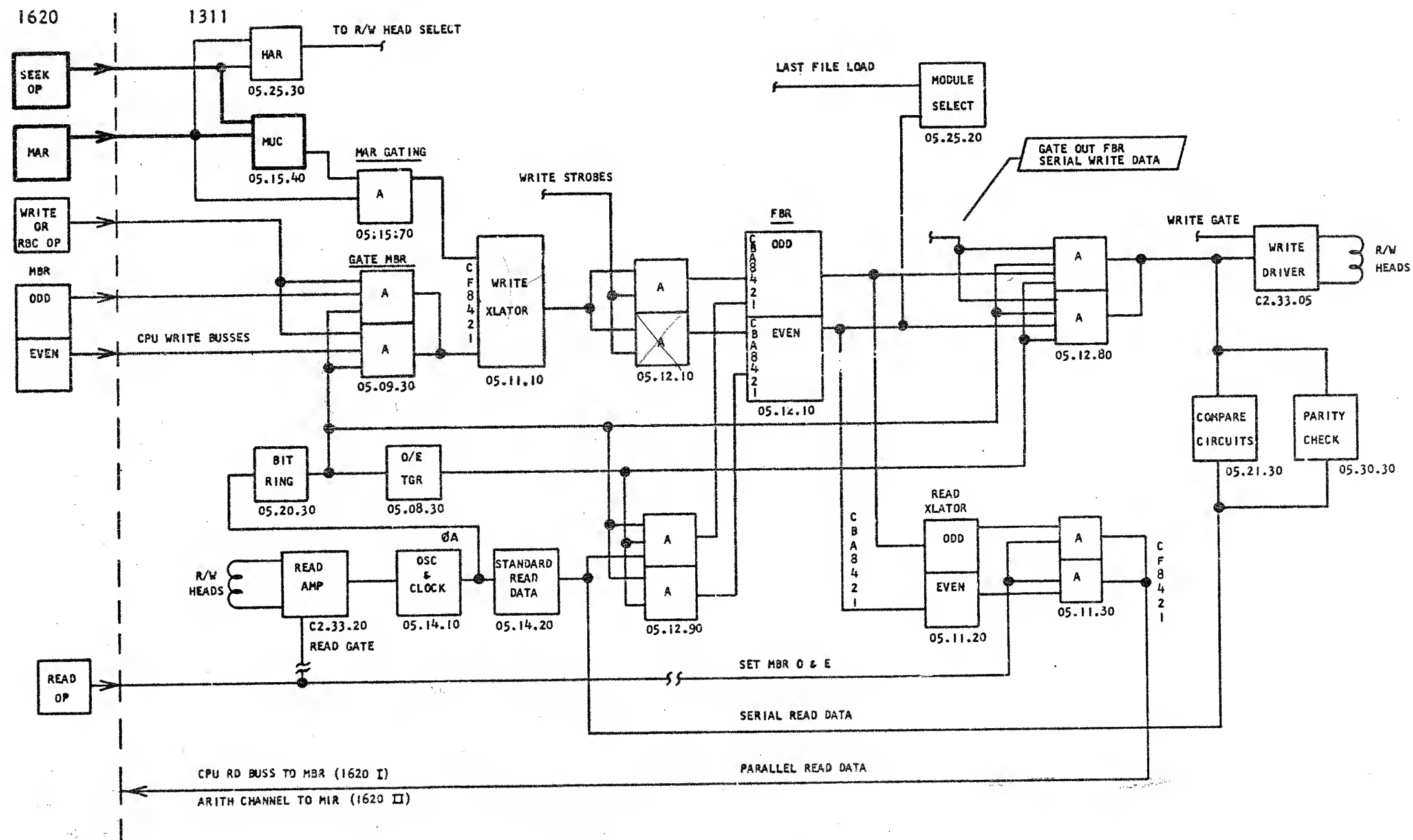






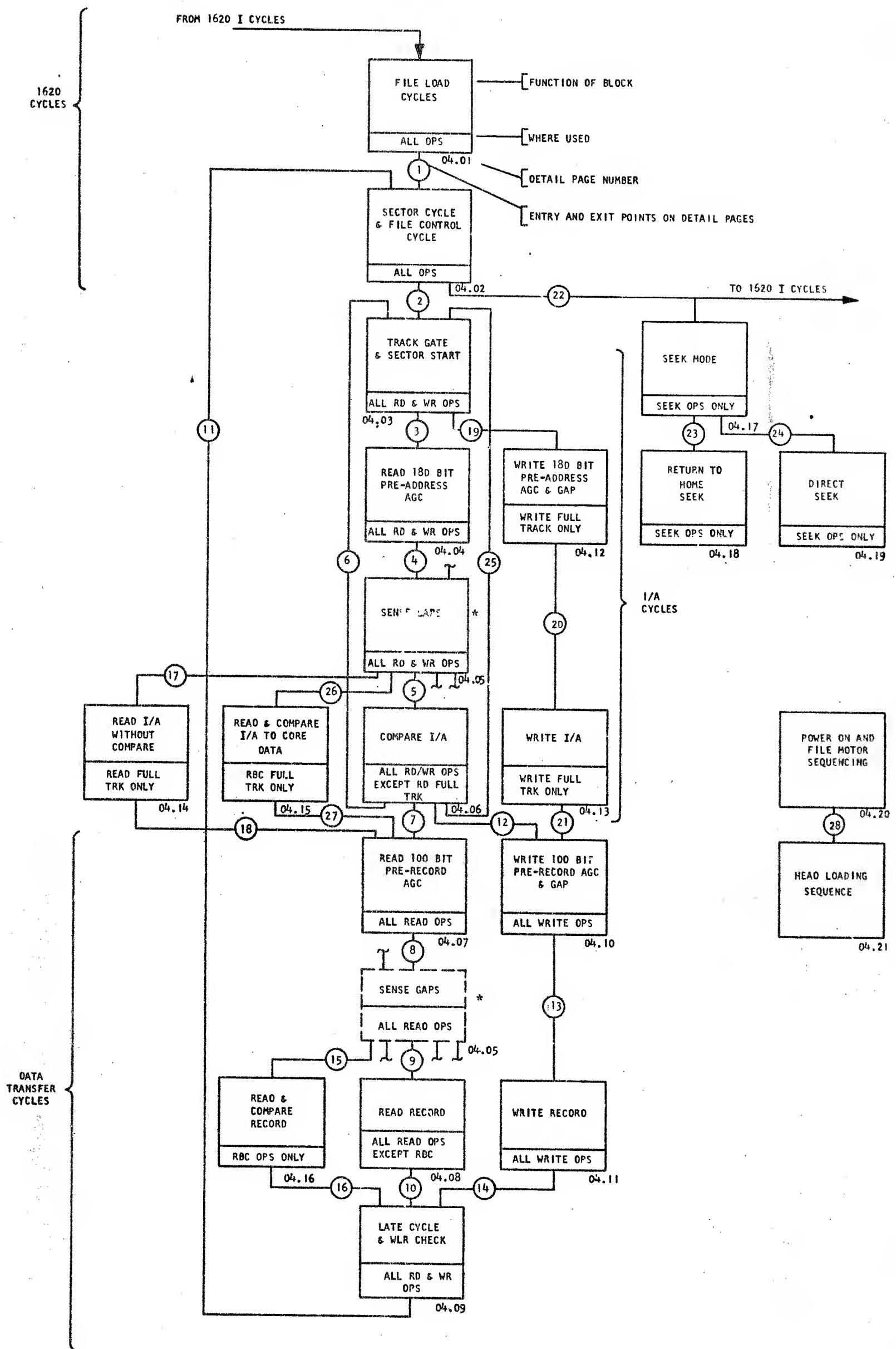




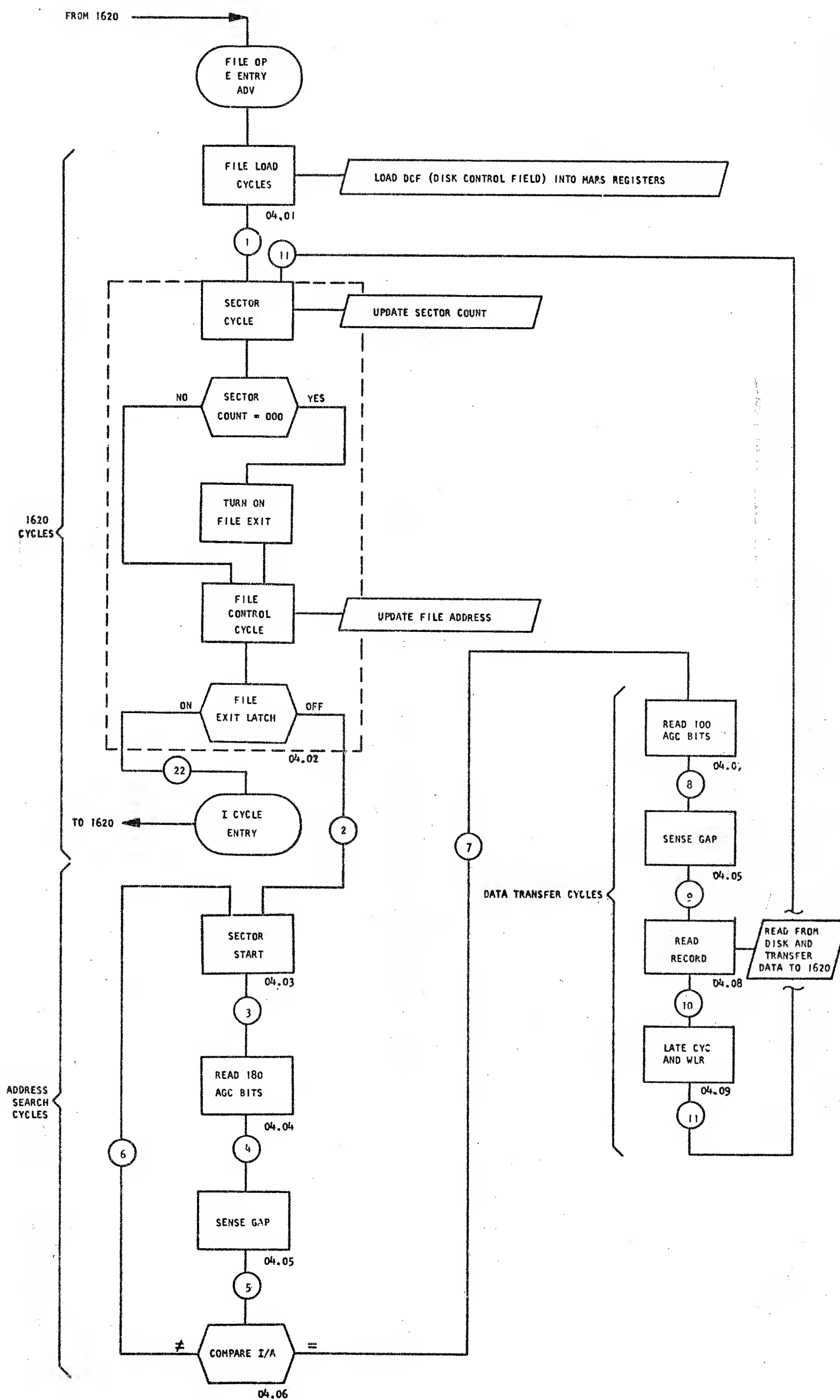


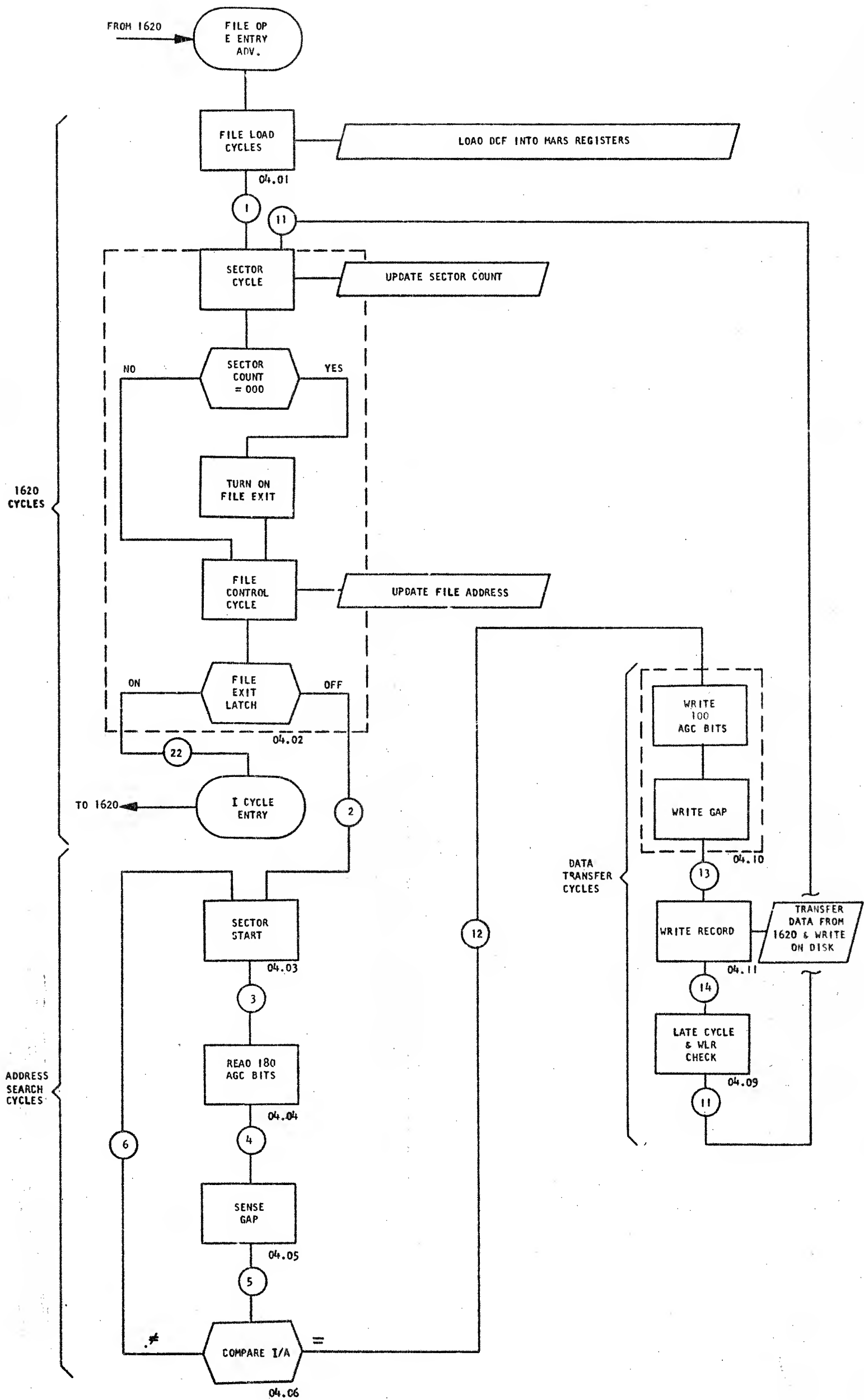
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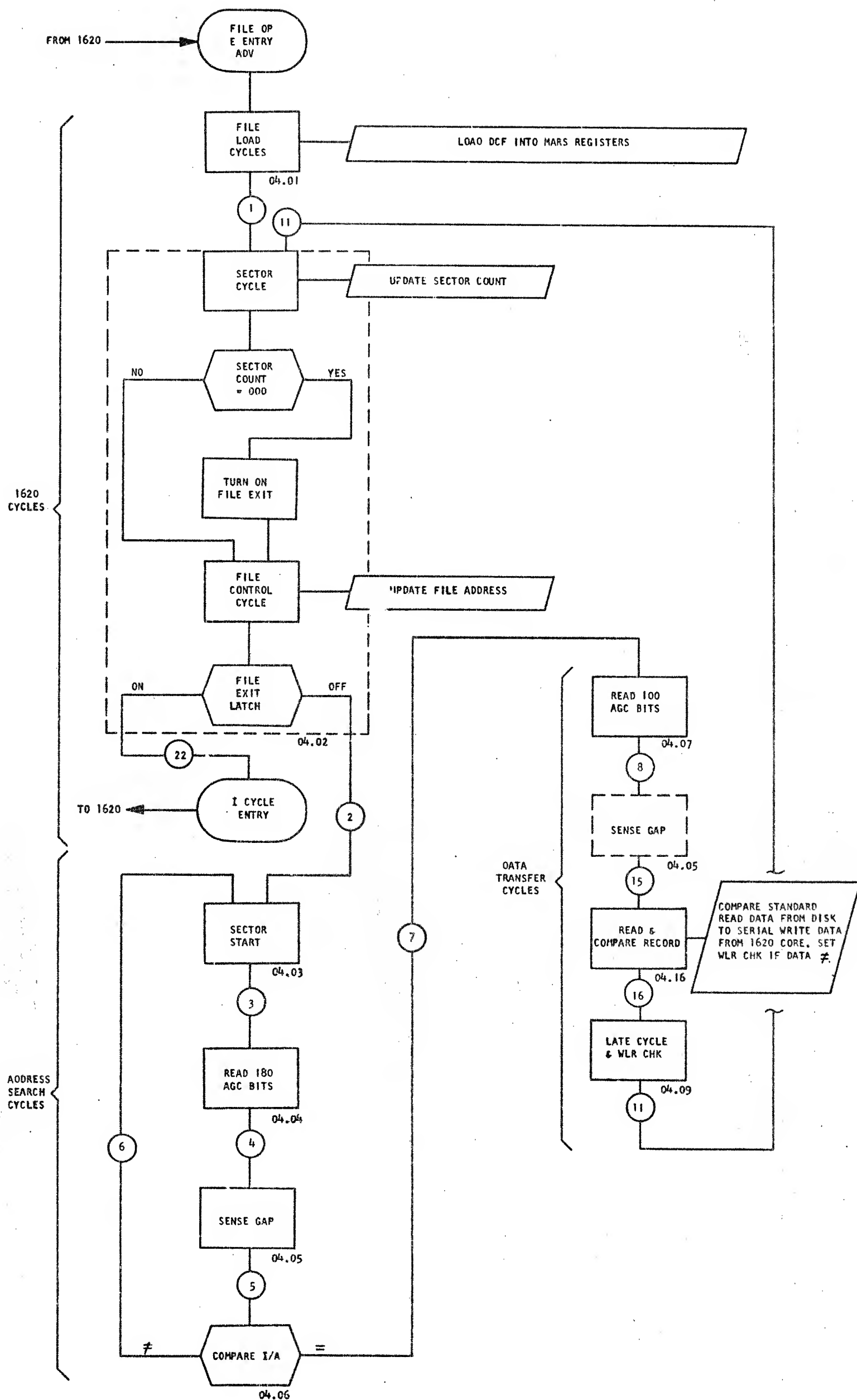
FILE OPERATIONAL UNITS	03.01
SECTOR OPERATIONS	
READ SECTOR OP	03.02
WRITE SECTOR OP	03.03
RBC SECTOR OP	03.04
TRACK OPERATIONS	
READ FULL TRACK	03.05
WRITE FULL TRACK WITH ADDRESSES	03.06
READ BACK CHECK FULL TRACK	03.07
SEEK OPERATIONS	03.08

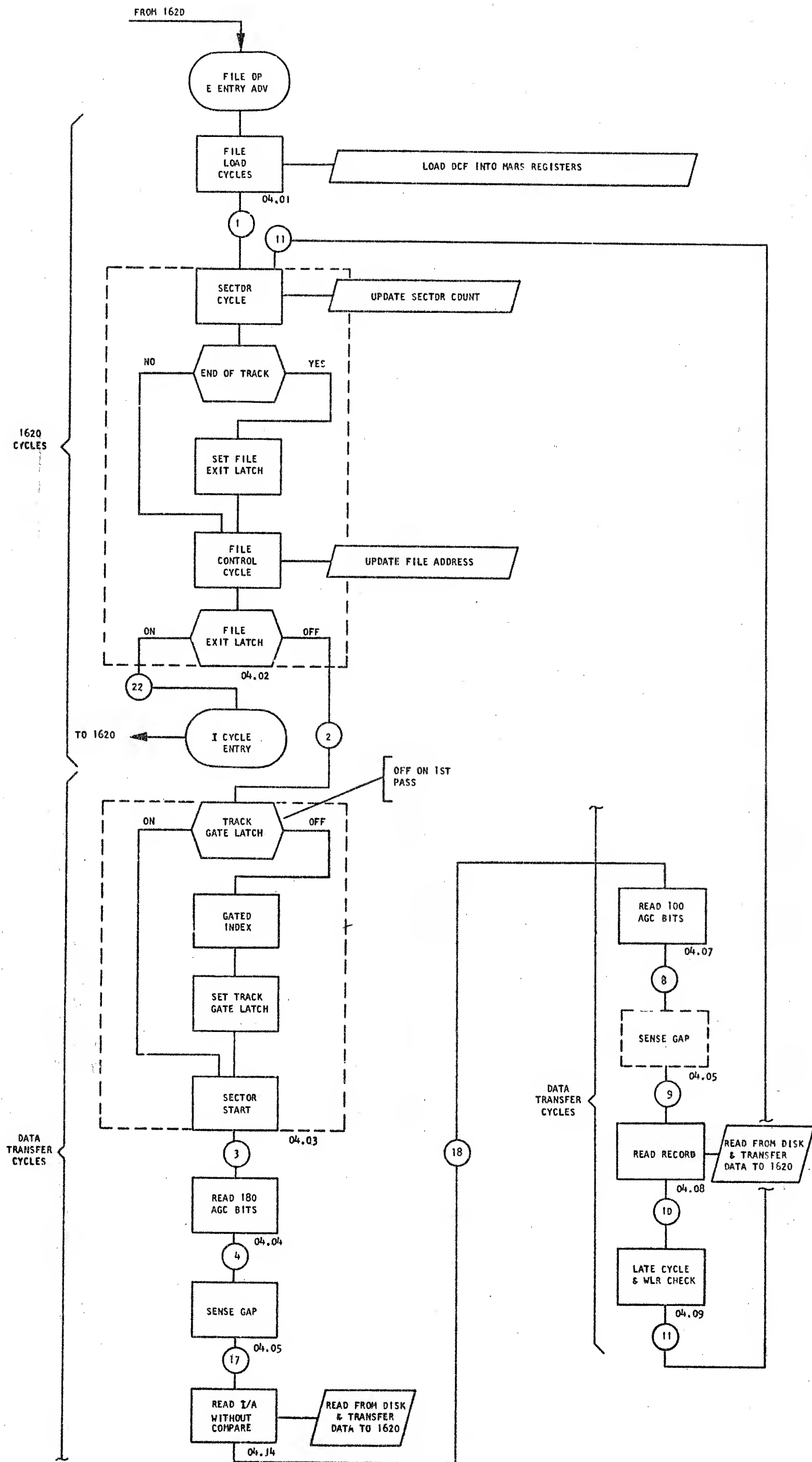


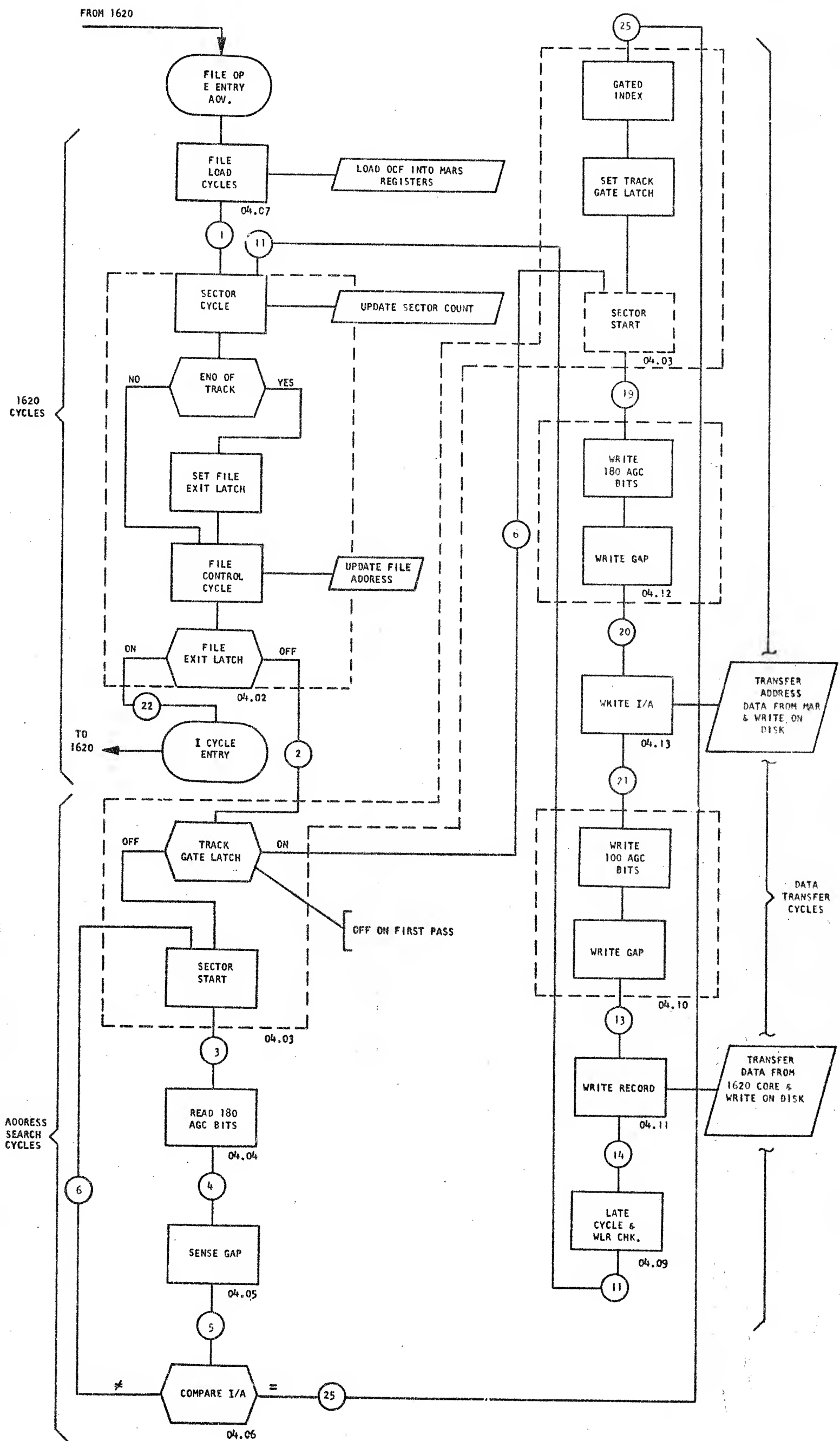
* BLOCK 04.05 SHOWN TWICE



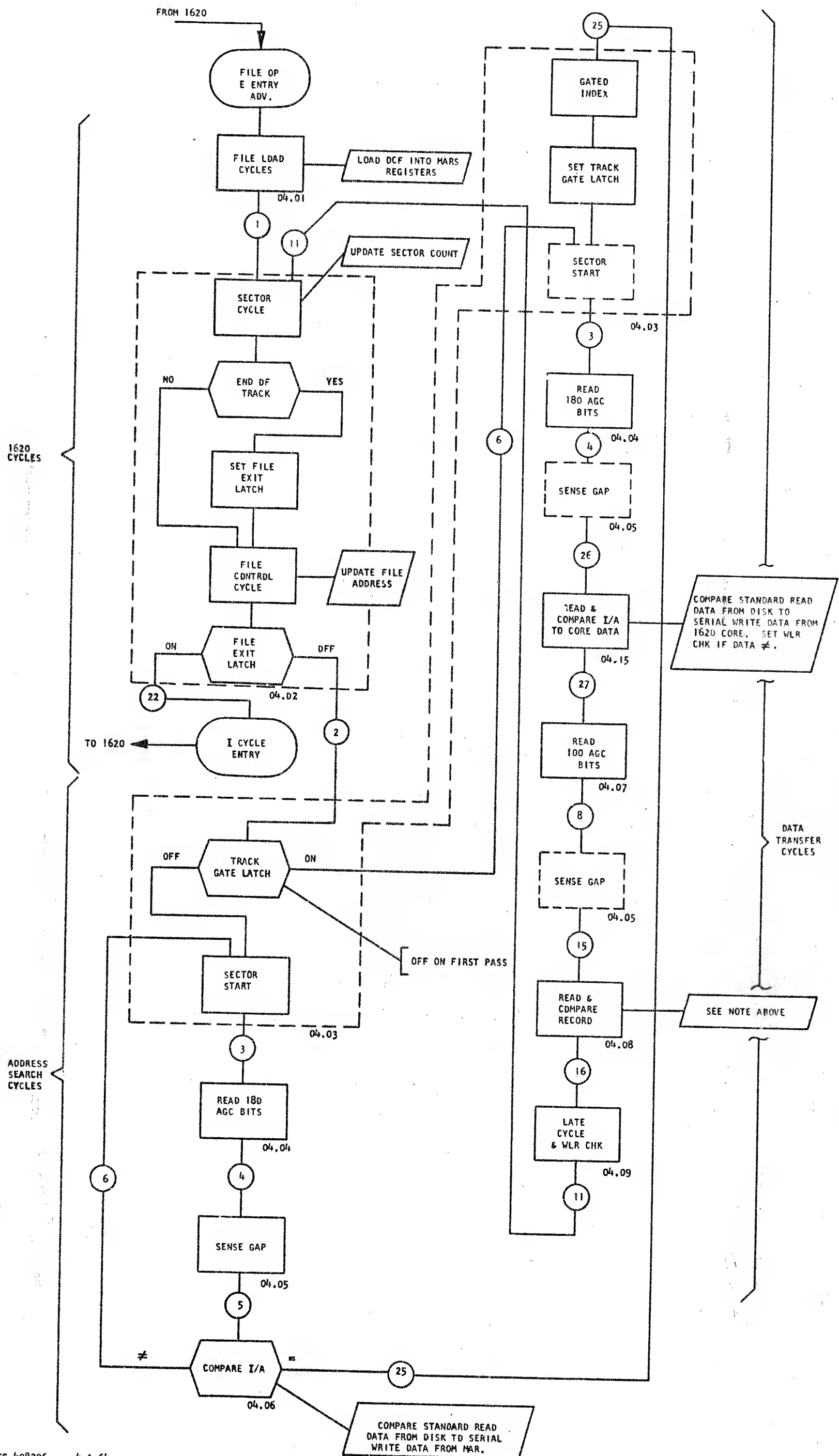


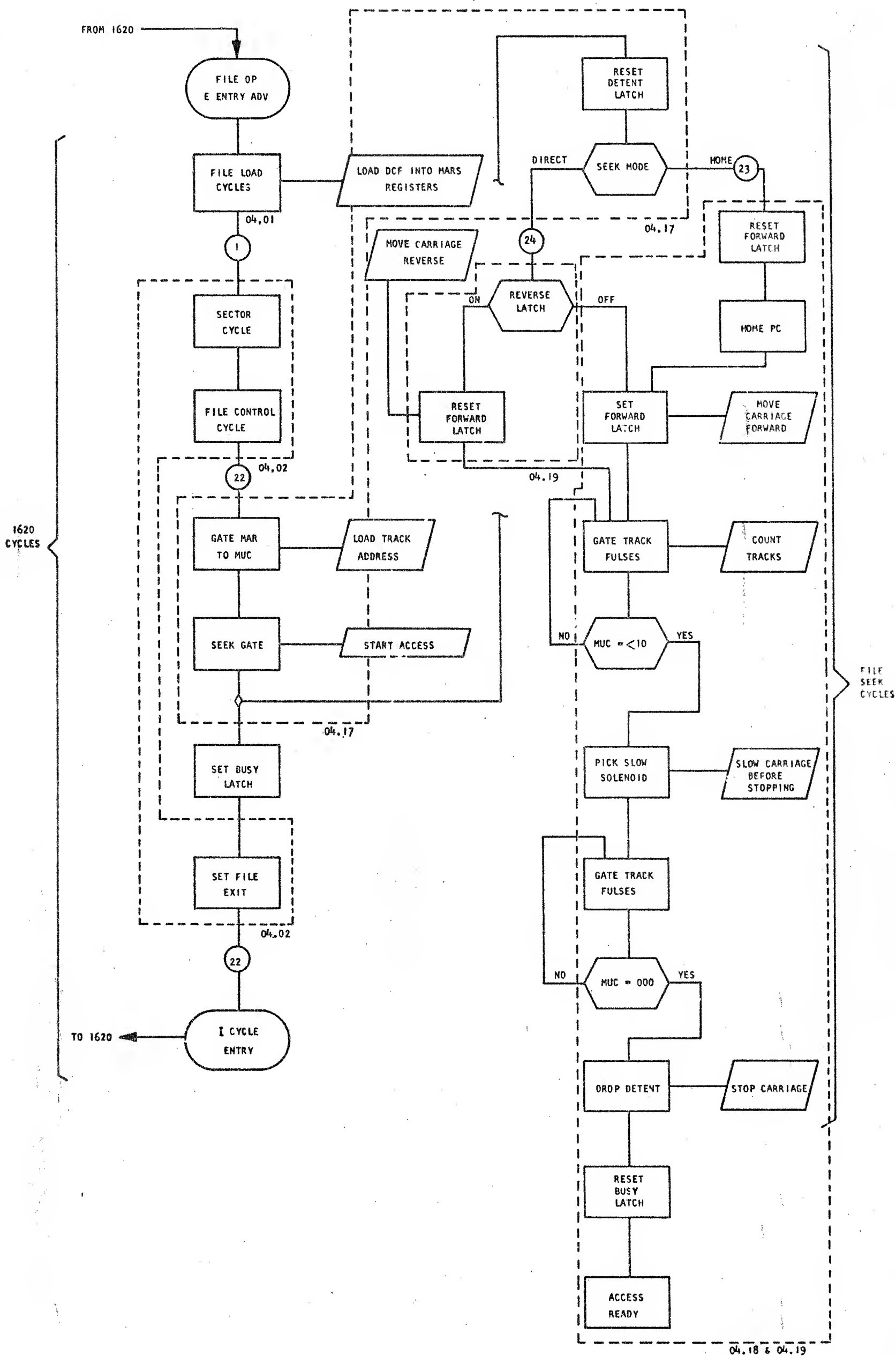






* WRITE ADDRESS SWITCH ON





INDEX

1620 CYCLES

FILE LOAD CYCLES	04.01
SECTOR CYCLE, FILE CONTROL CYCLE	04.02

ADDRESS SEARCH CYCLES

TRACK GATE & SECTOR START	04.03
READ 180 BIT PRE-ADDRESS AGC	04.04
SENSE GAPS	04.05
COMPARE I/A	04.06

DATA TRANSFER CYCLES

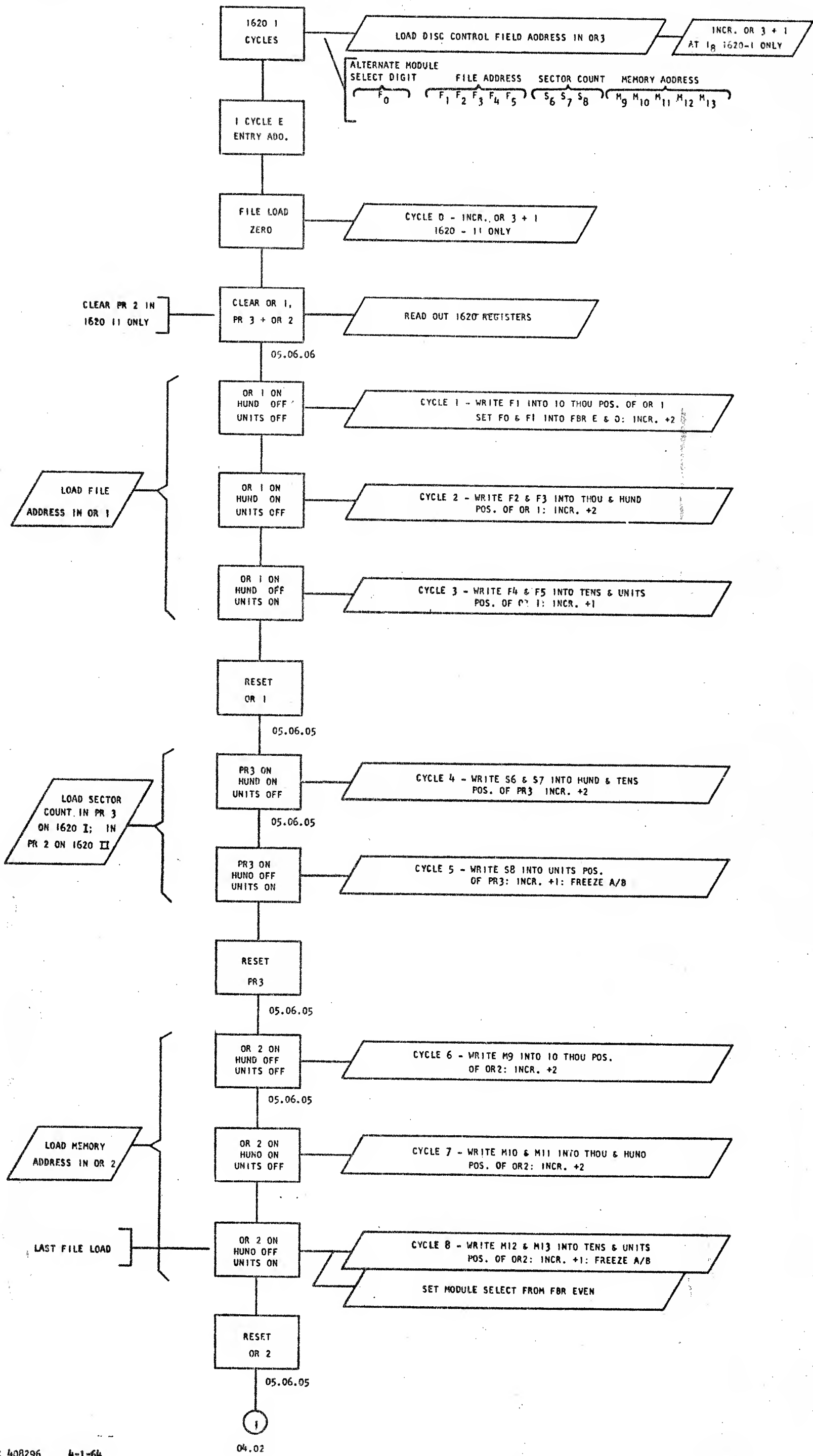
READ 100 BIT PRE-RECORD AGC	04.07
READ RECORD	04.08
READ I/A WITHOUT COMPARE	04.14
READ & COMPARE I/A TO CORE DATA	04.15
READ & COMPARE RECORD	04.16
LATE CYCLE & WLR CHECK	04.09
WRITE 180 BIT PRE-ADDRESS AGC & GAP	04.12
WRITE INDELIBLE ADDRESS	04.13
WRITE 100 BIT PRE-RECORD AGC & GAP	04.10
WRITE RECORD	04.11

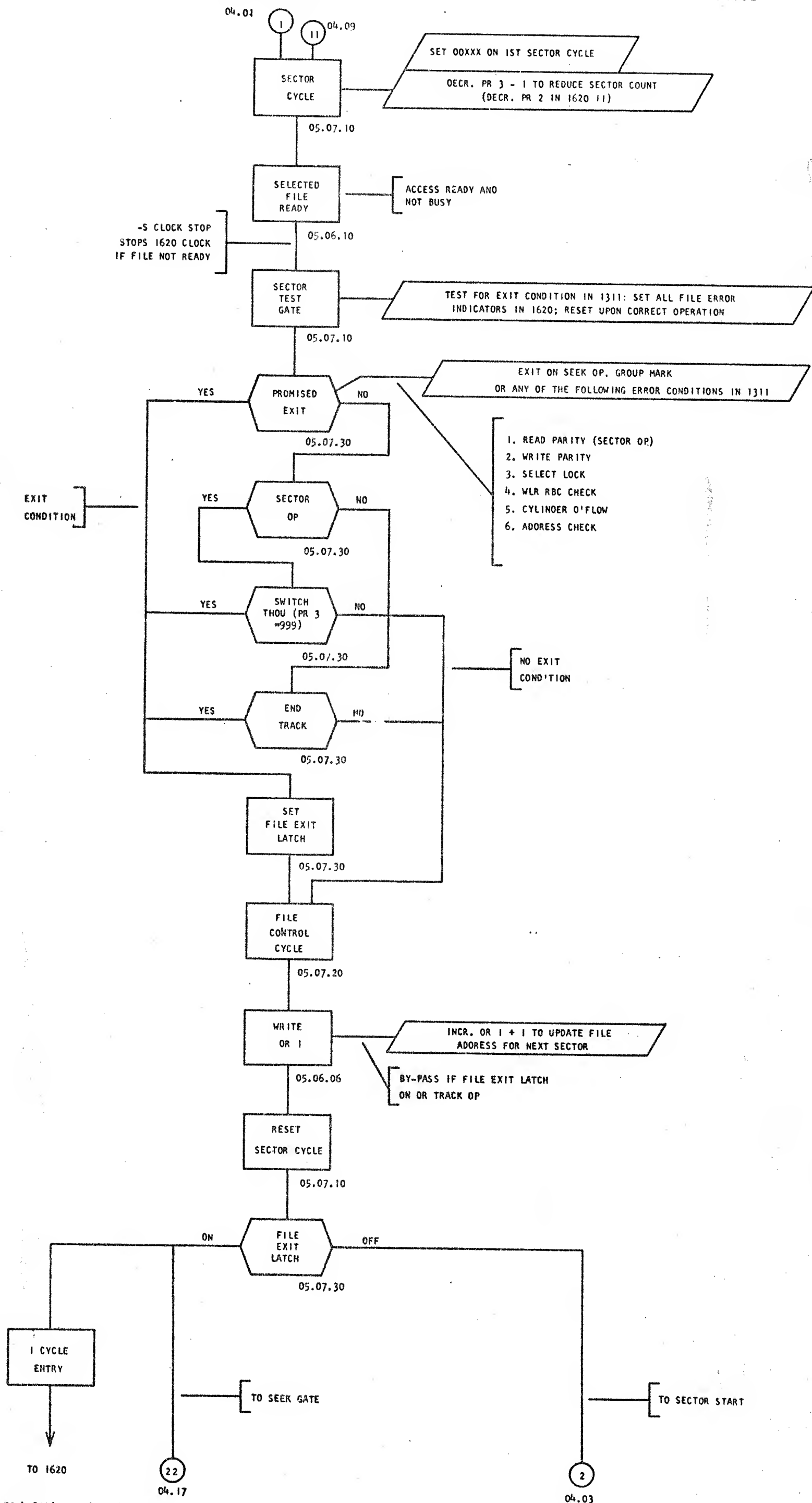
FILE SEEK CYCLES

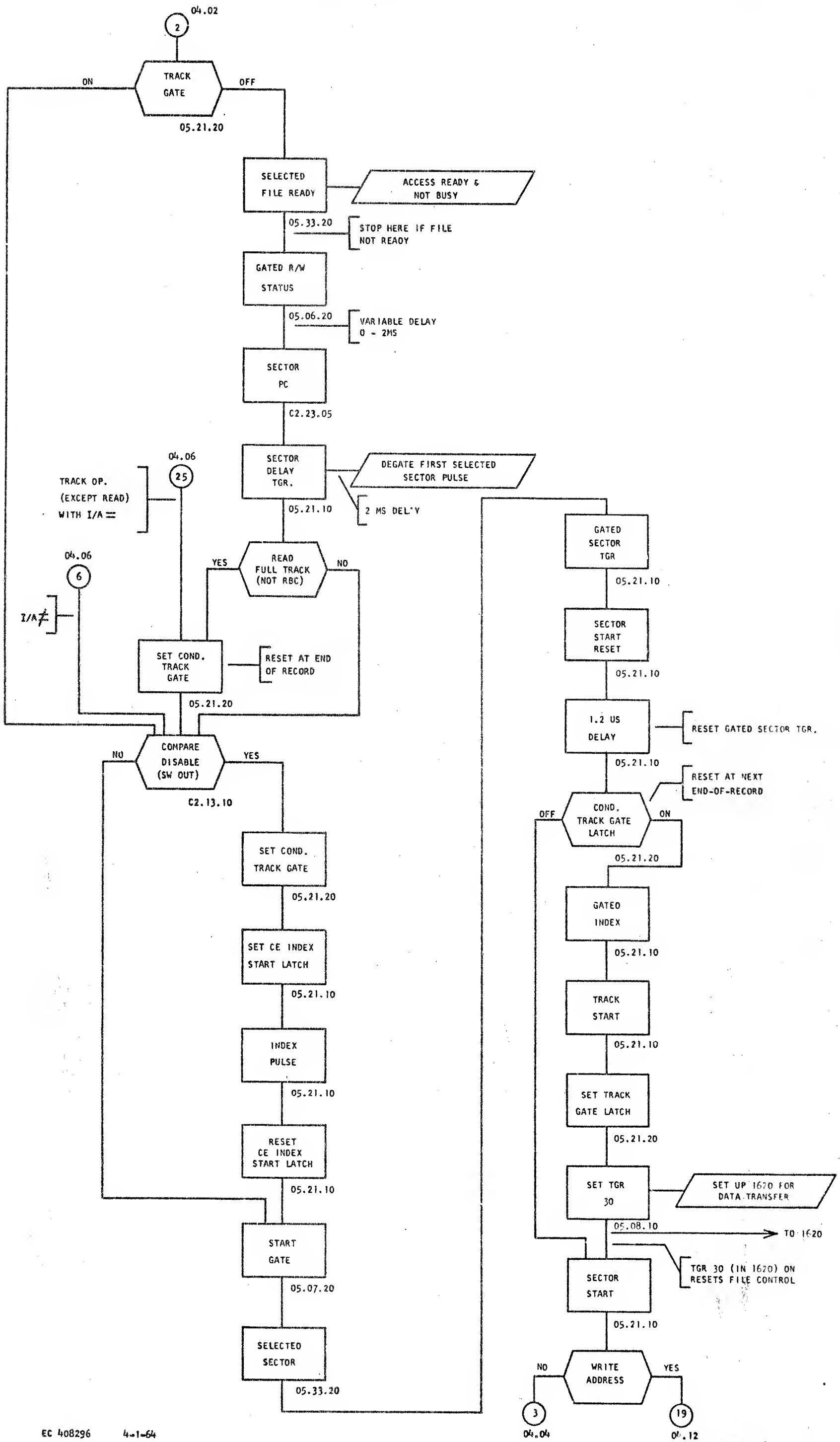
SEEK MODE	04.17
SEEK, RETURN TO HOME	04.18
SEEK, DIRECT	04.19

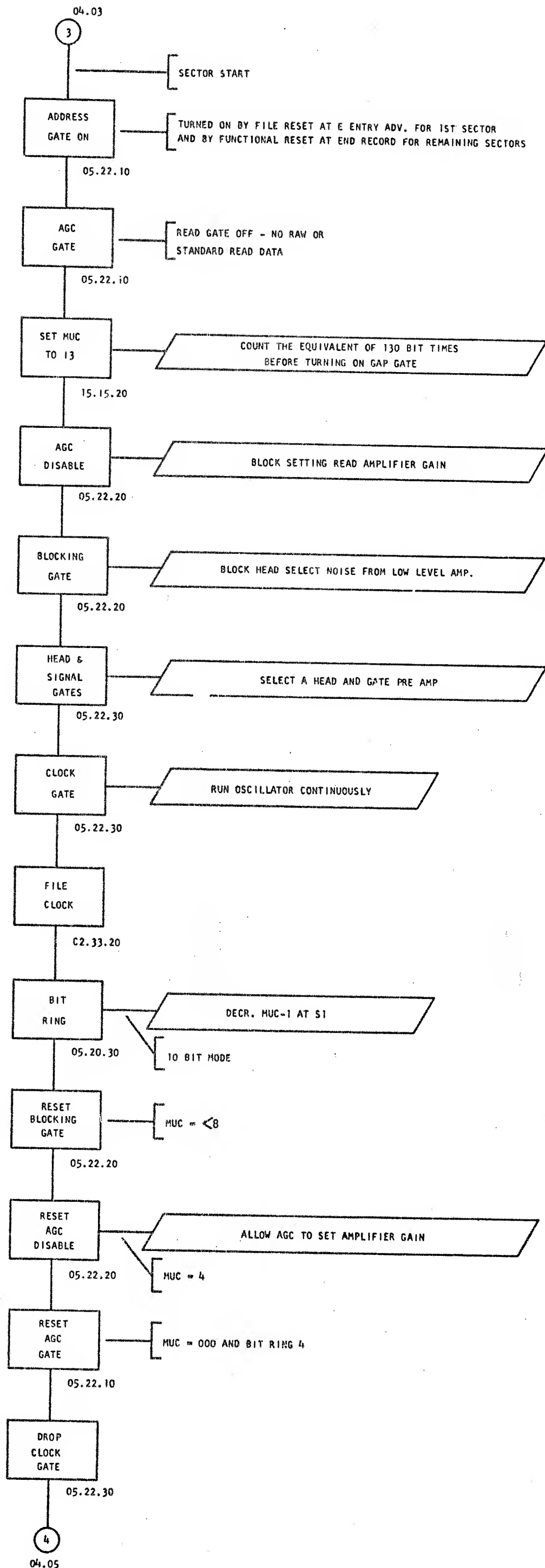
POWER-ON

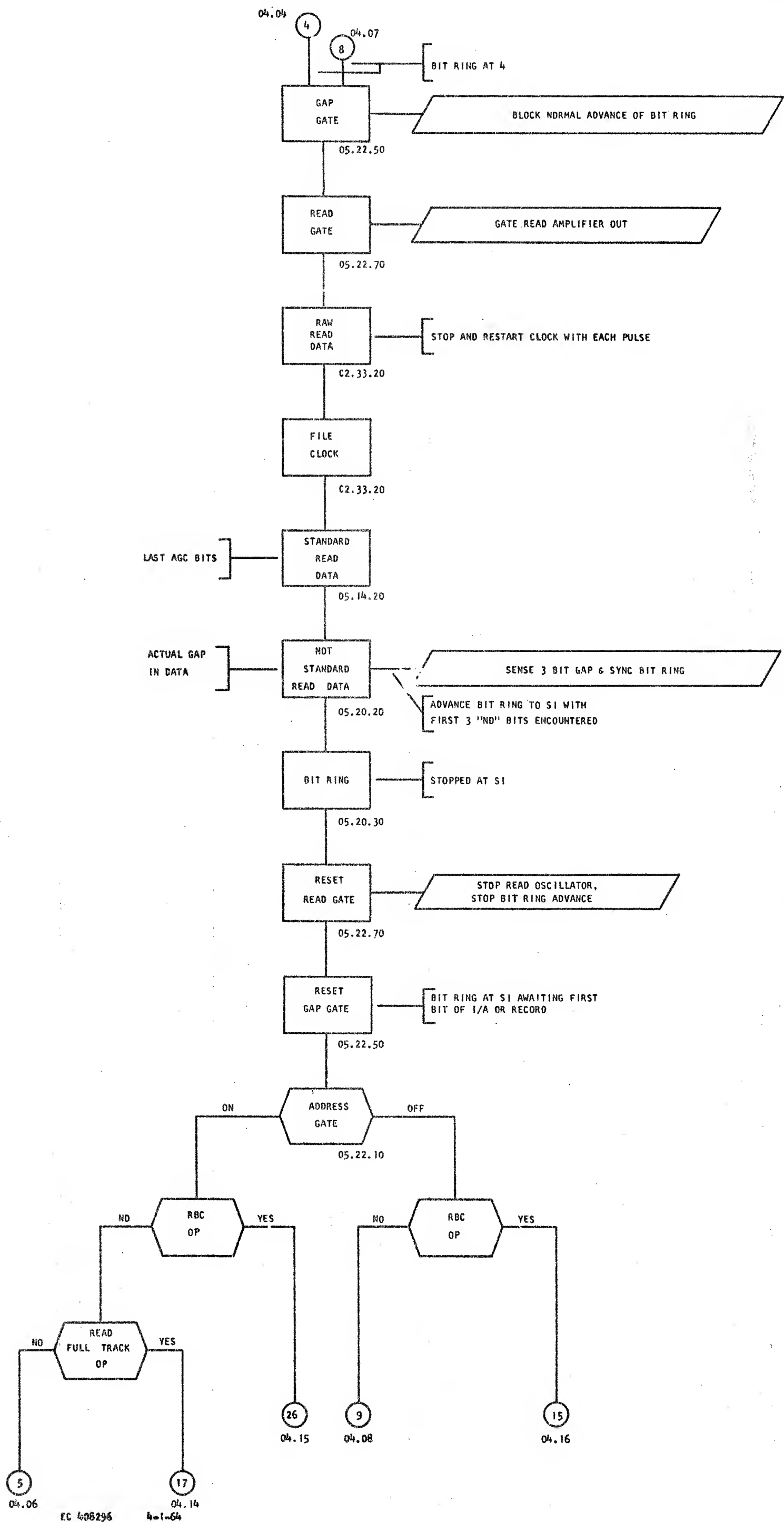
POWER ON & FILE MOTOR SEQUENCING	04.20
HEAD LOADING SEQUENCE	04.21

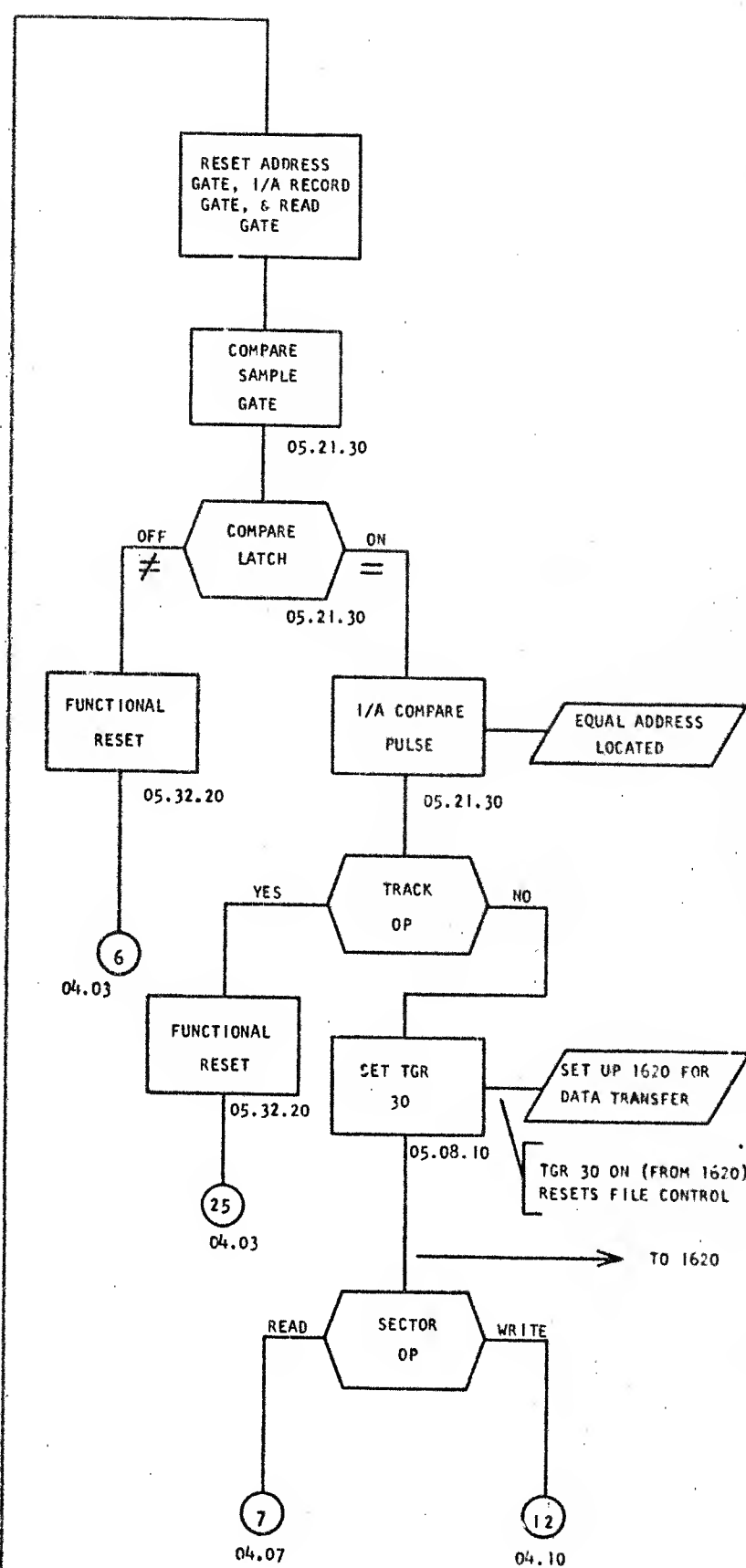
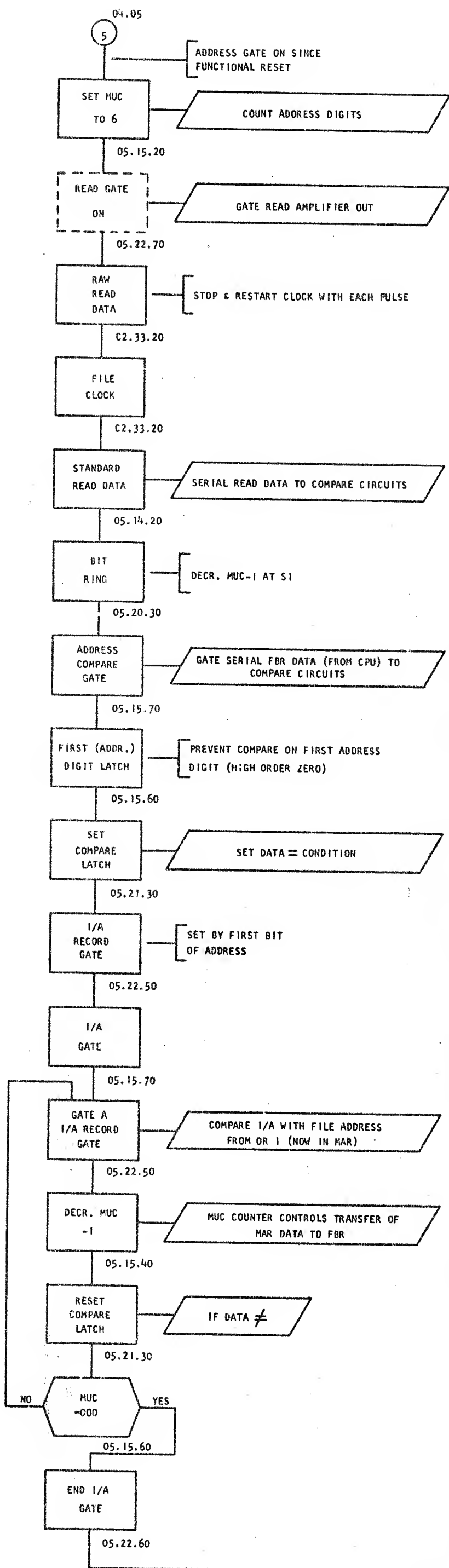


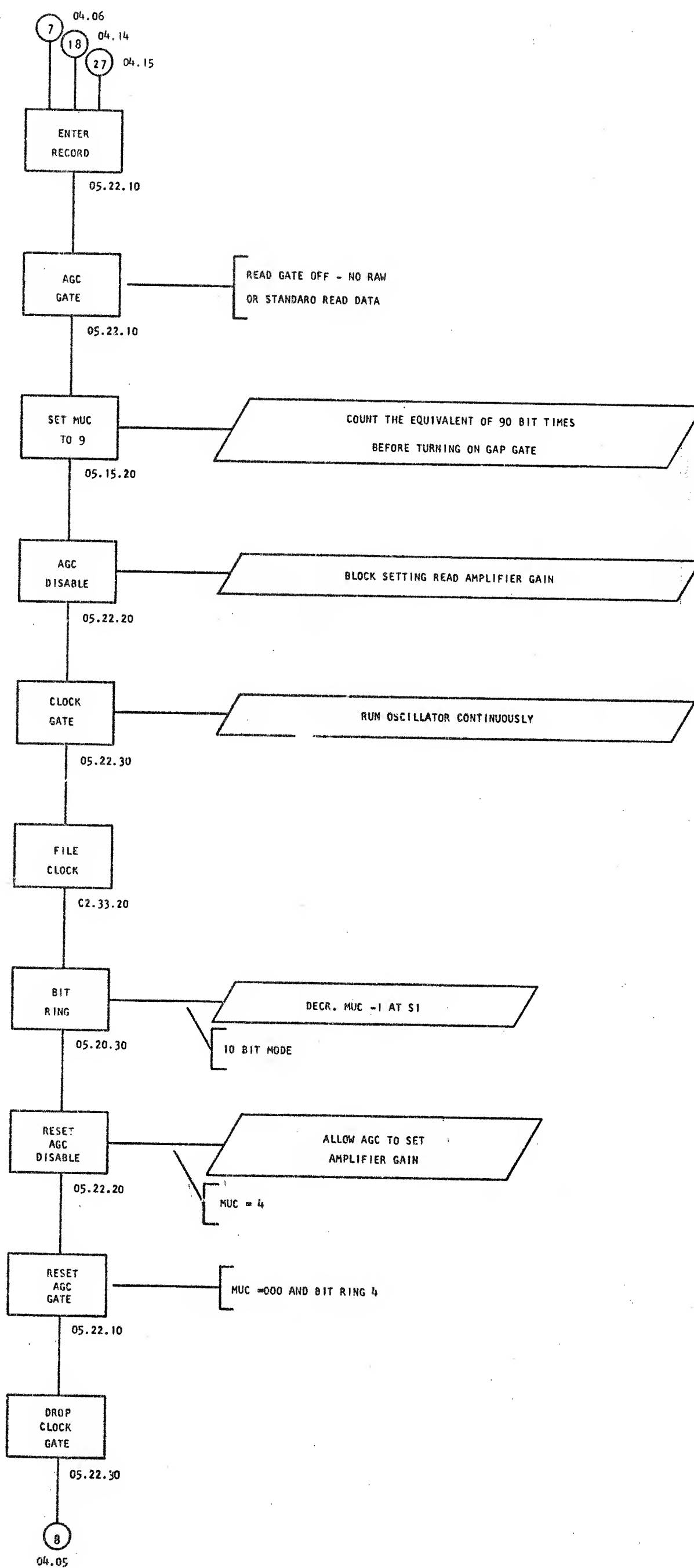


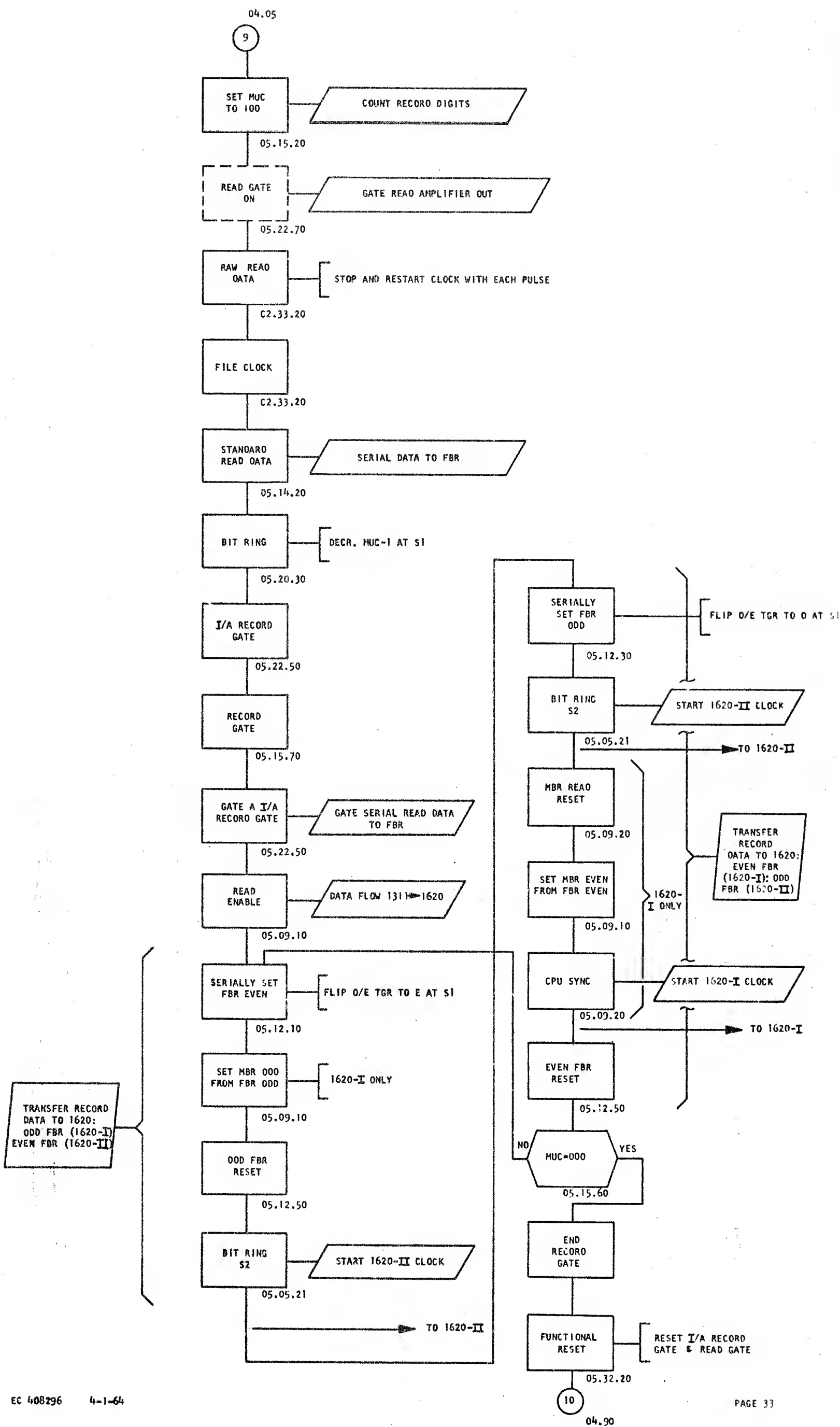


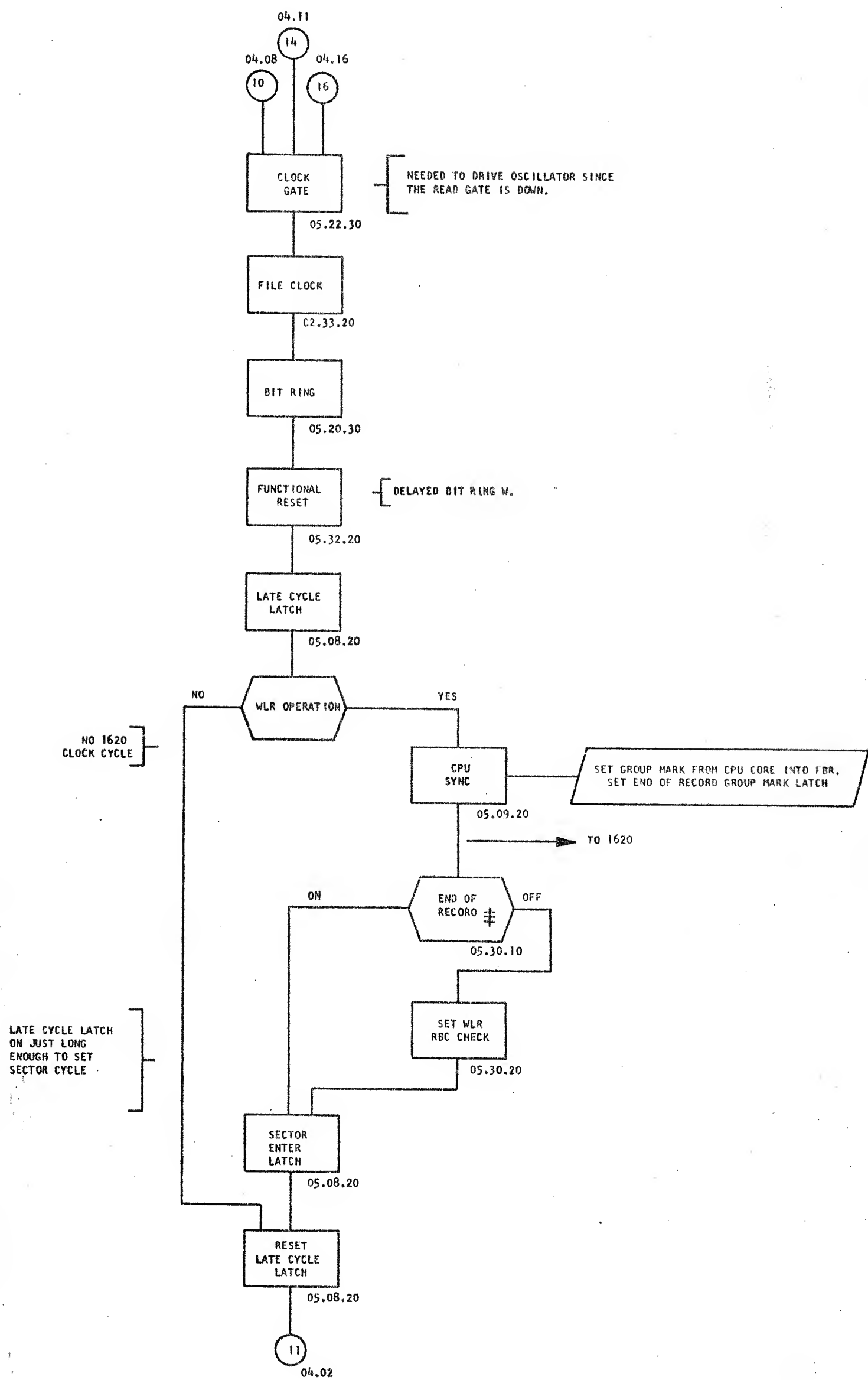


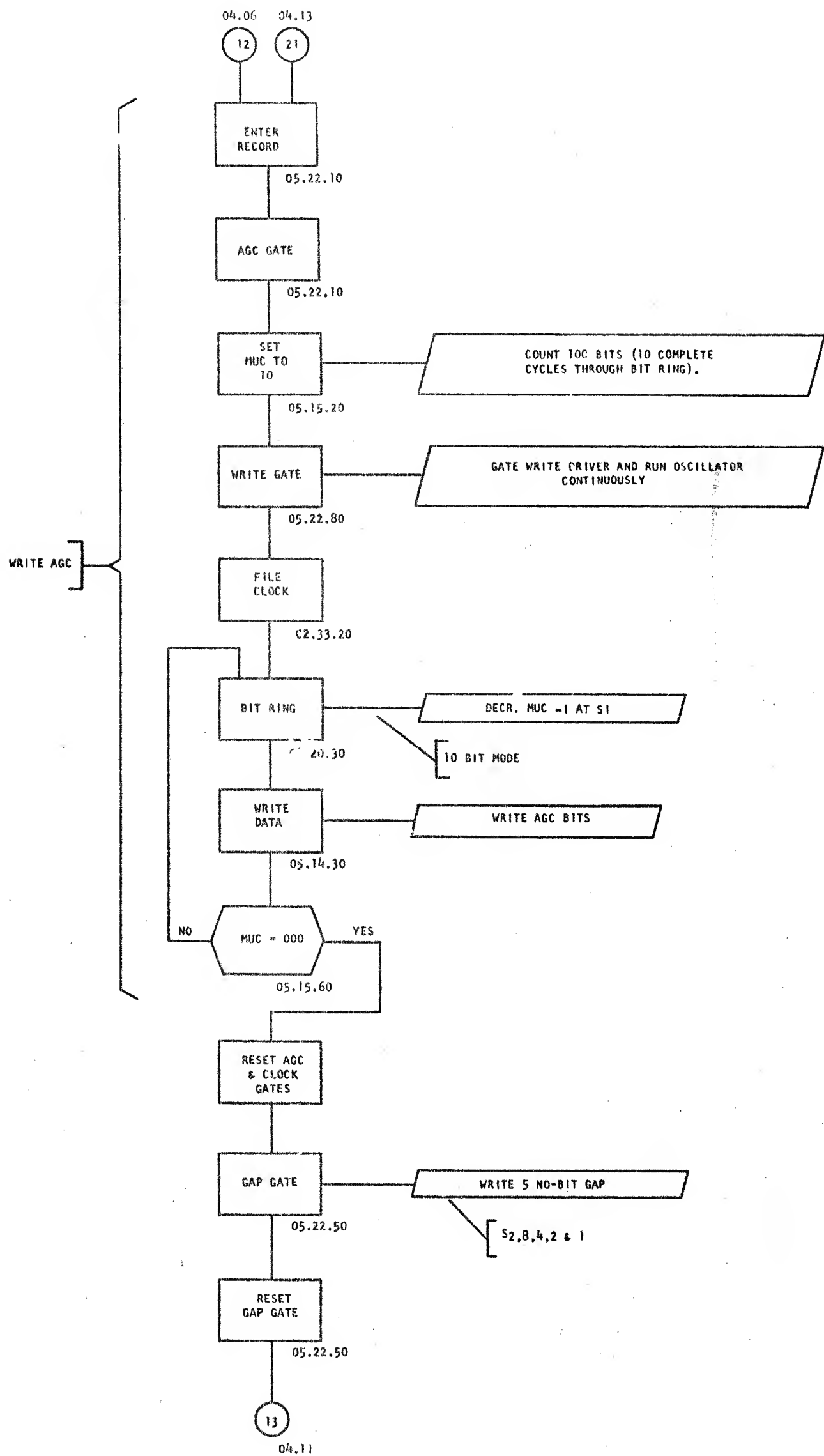


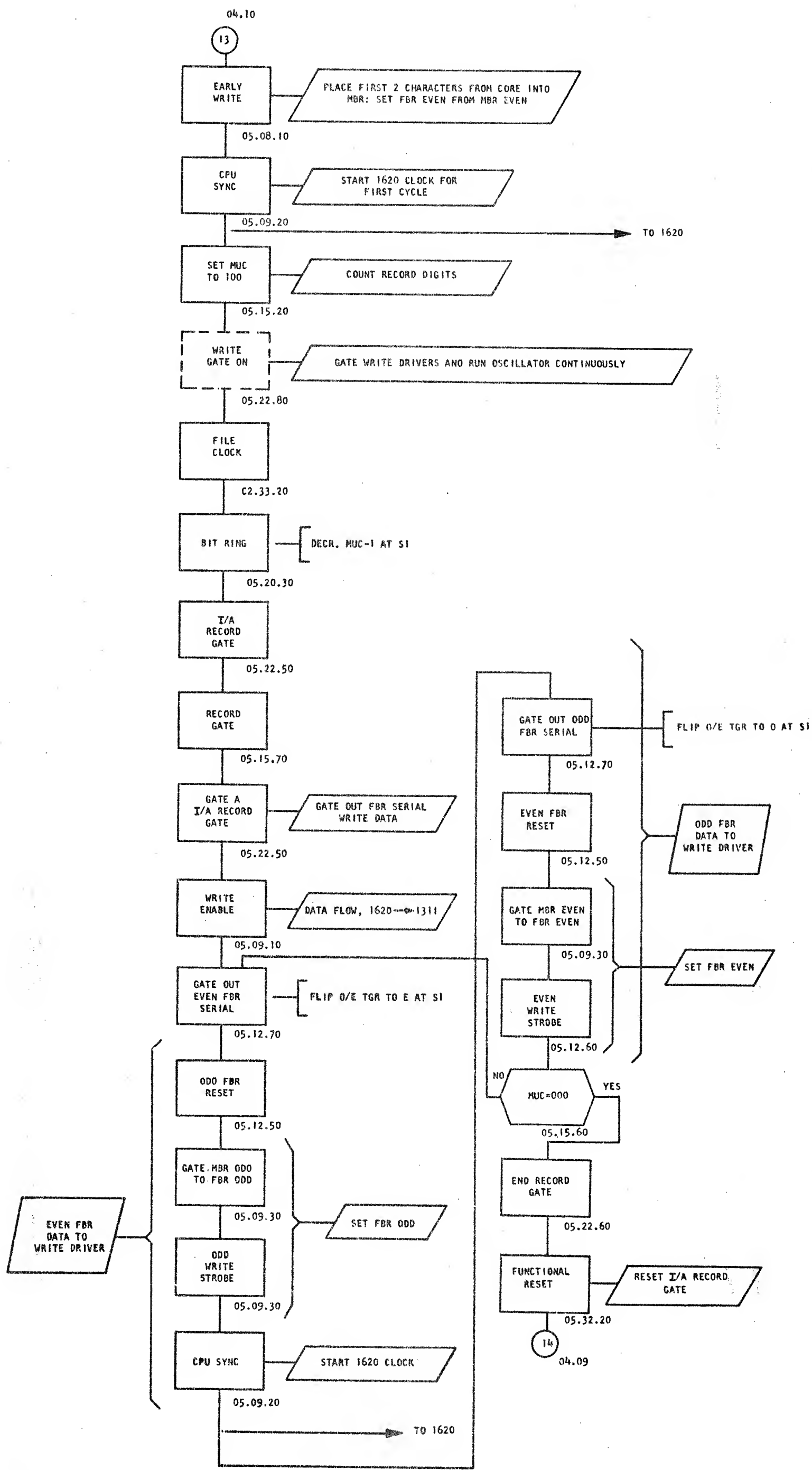


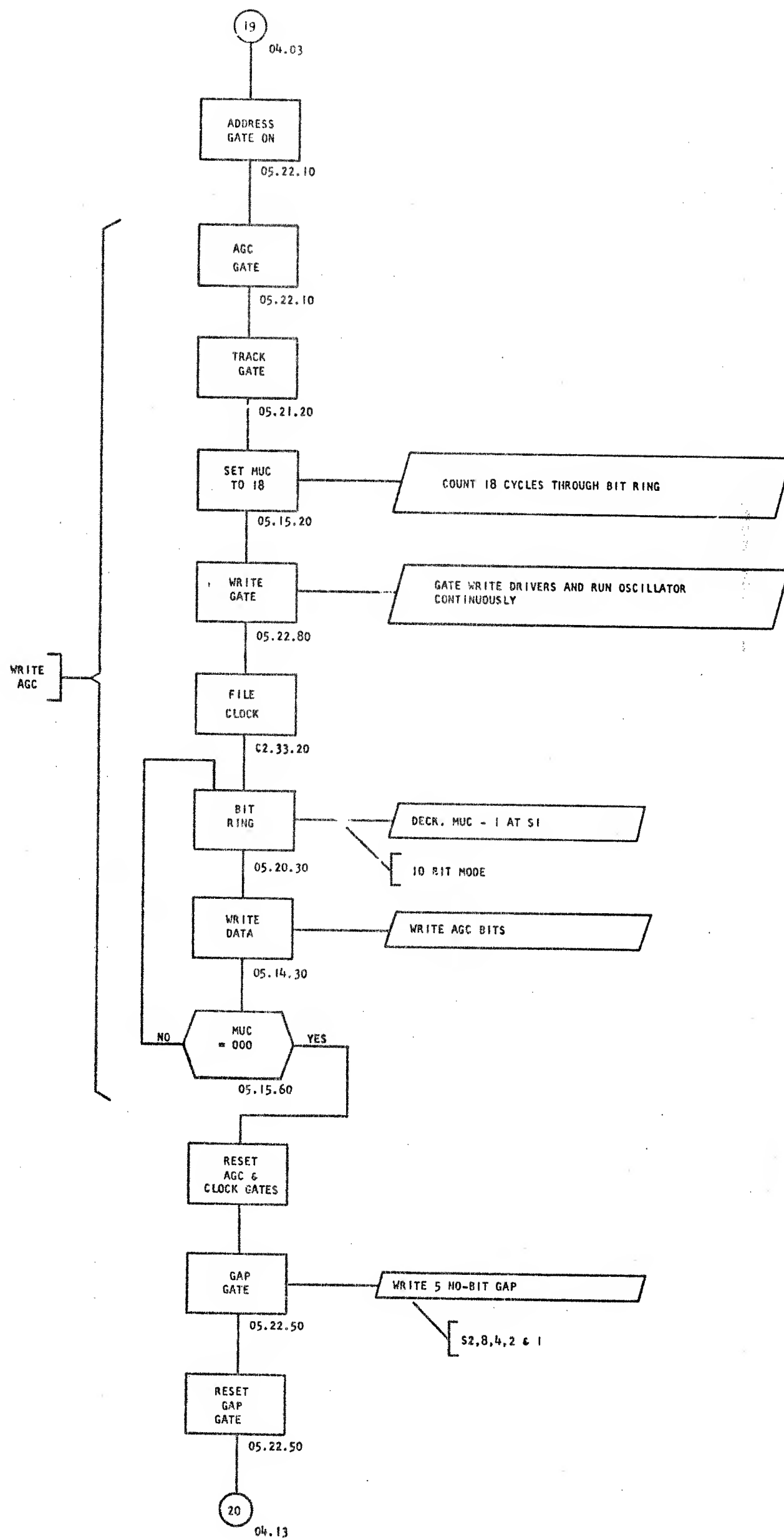


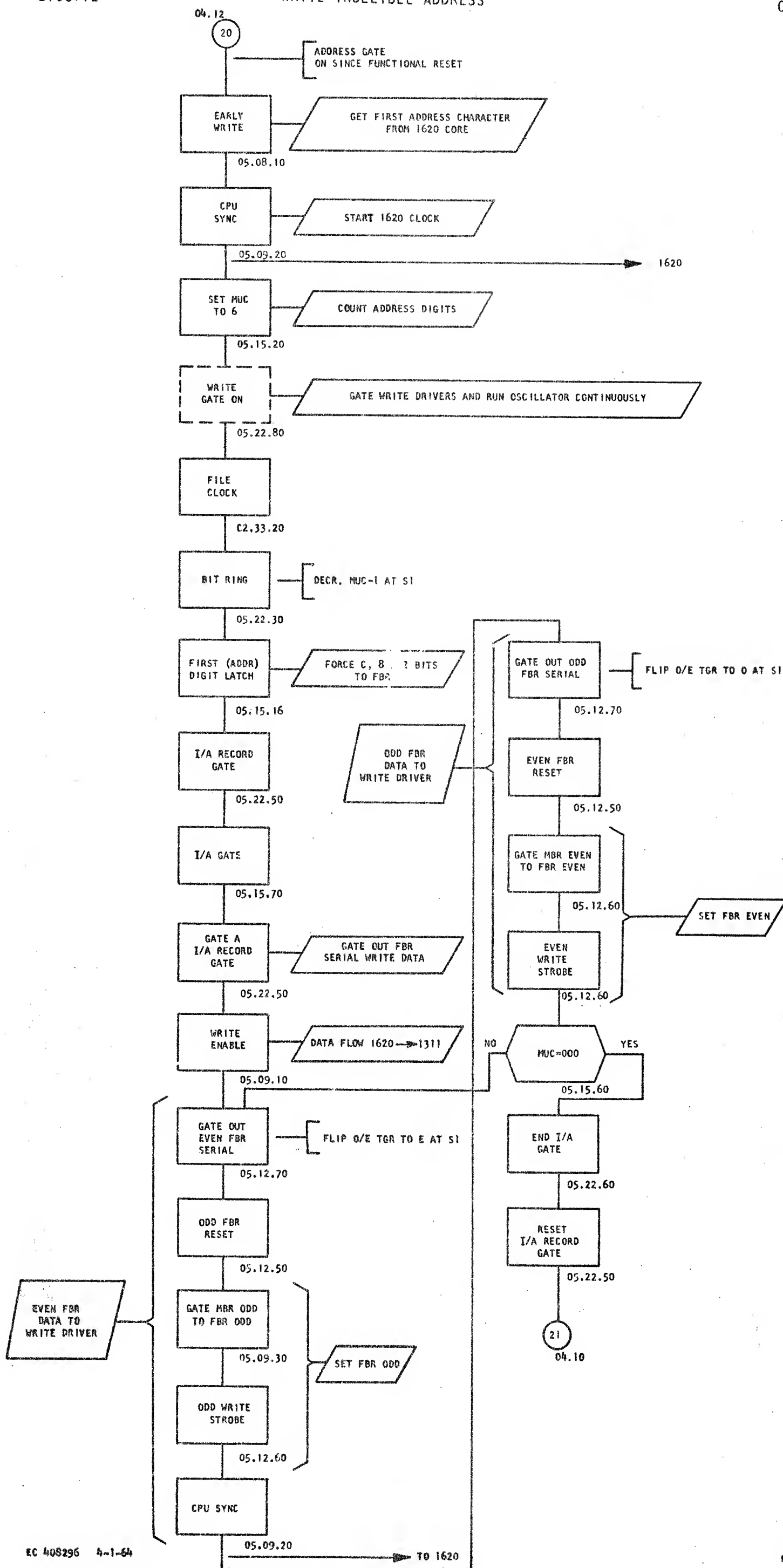


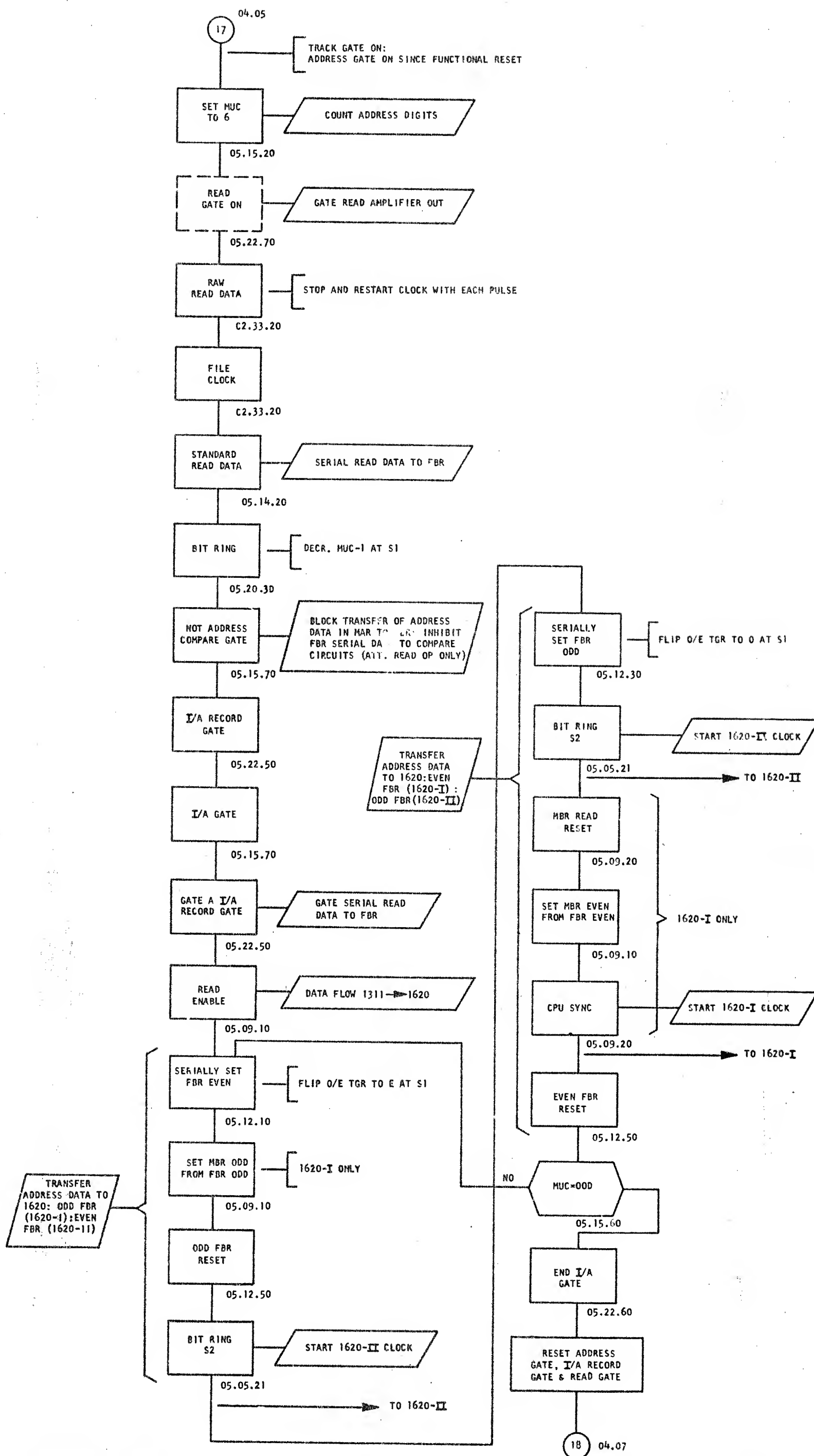


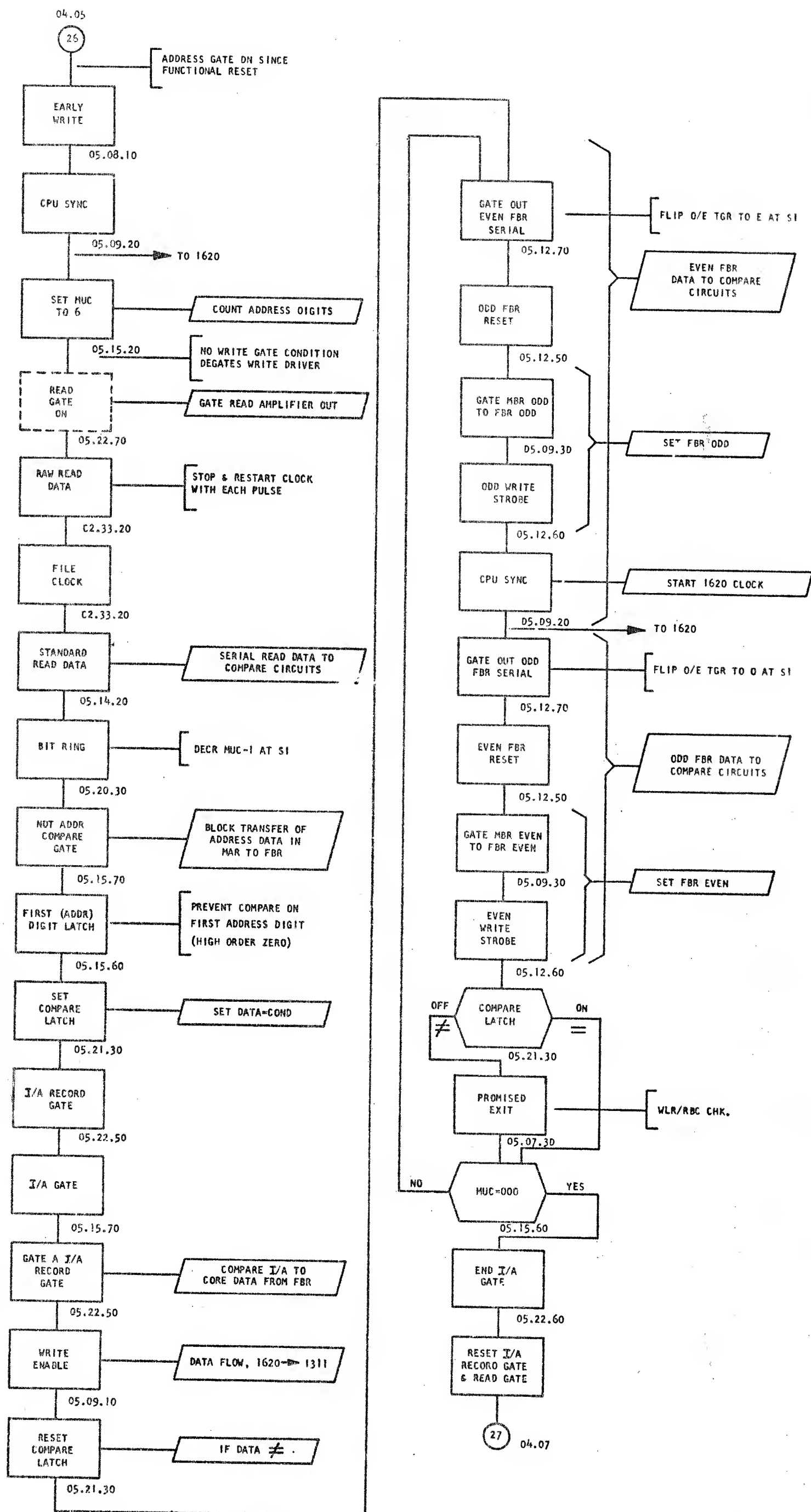


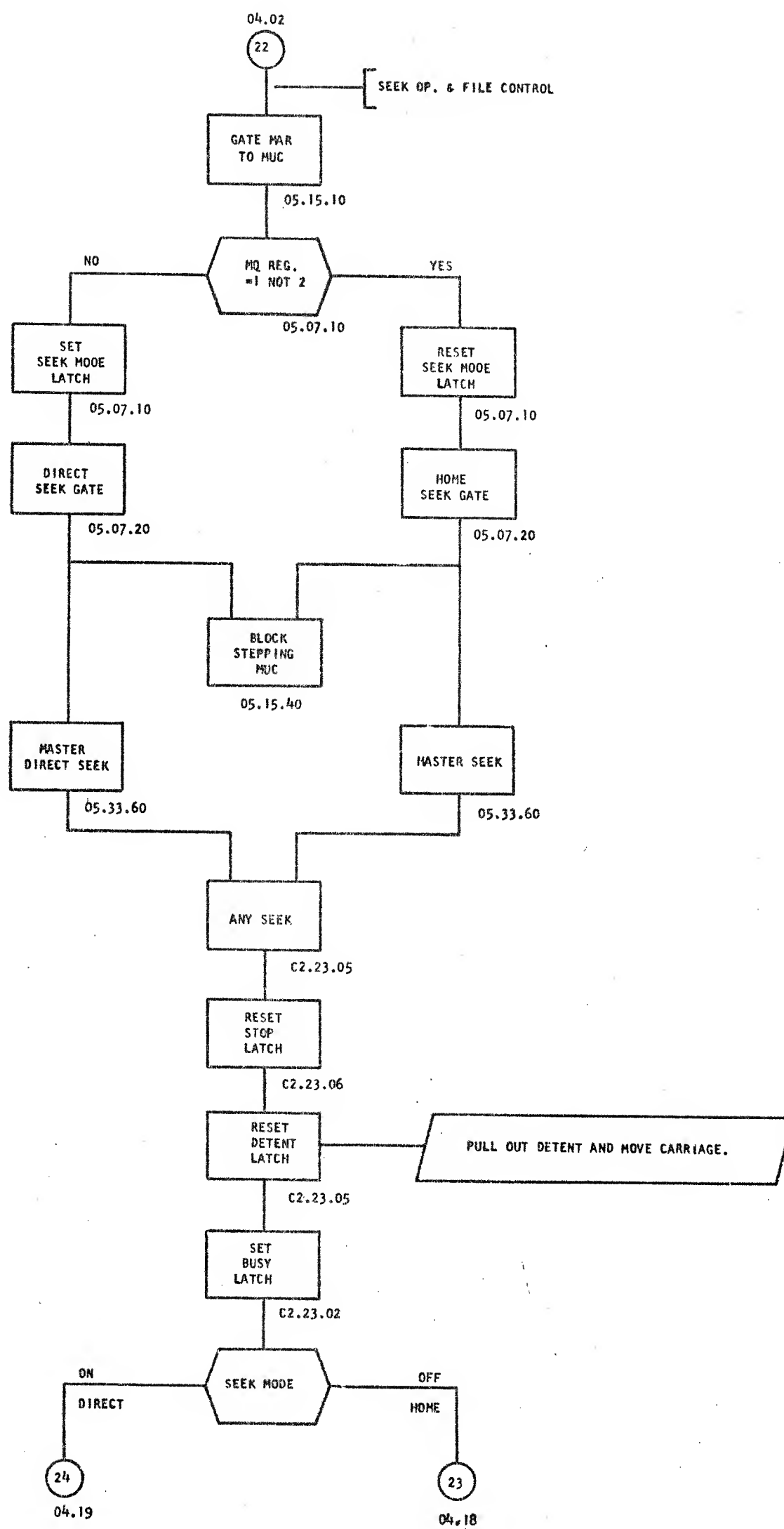


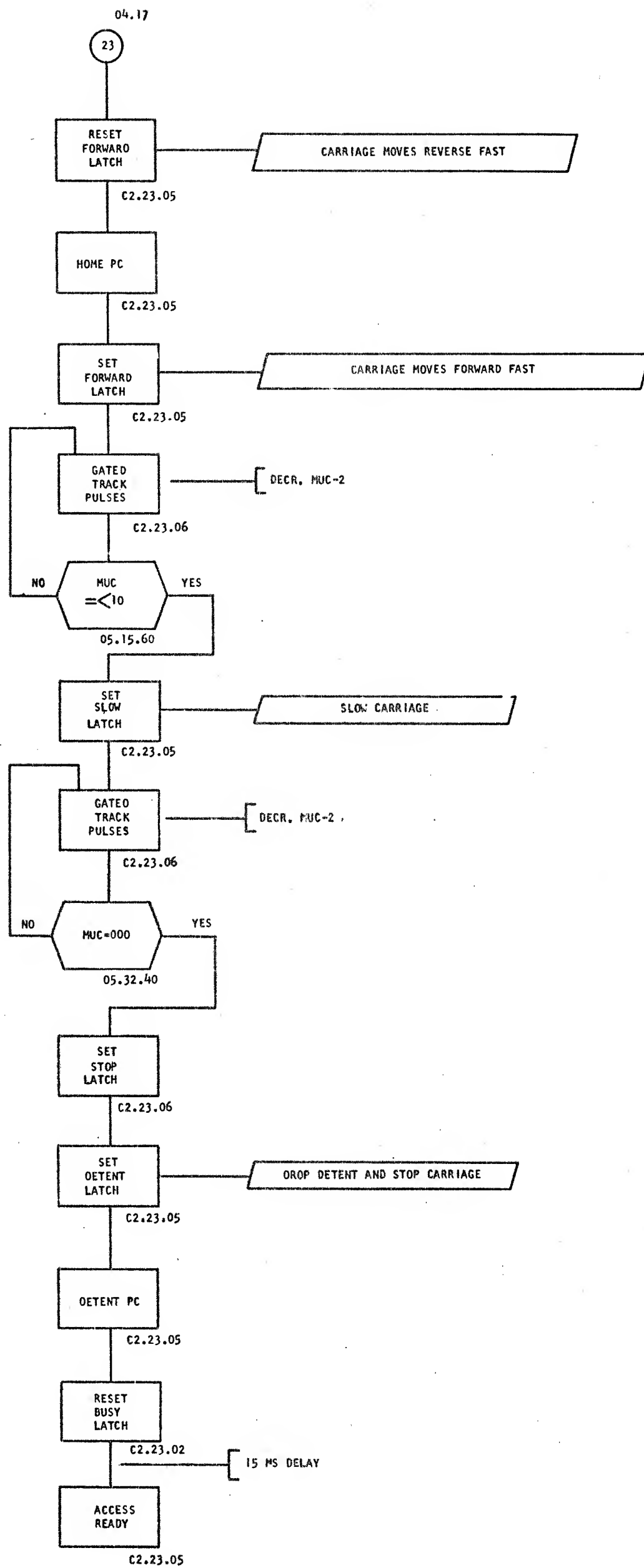


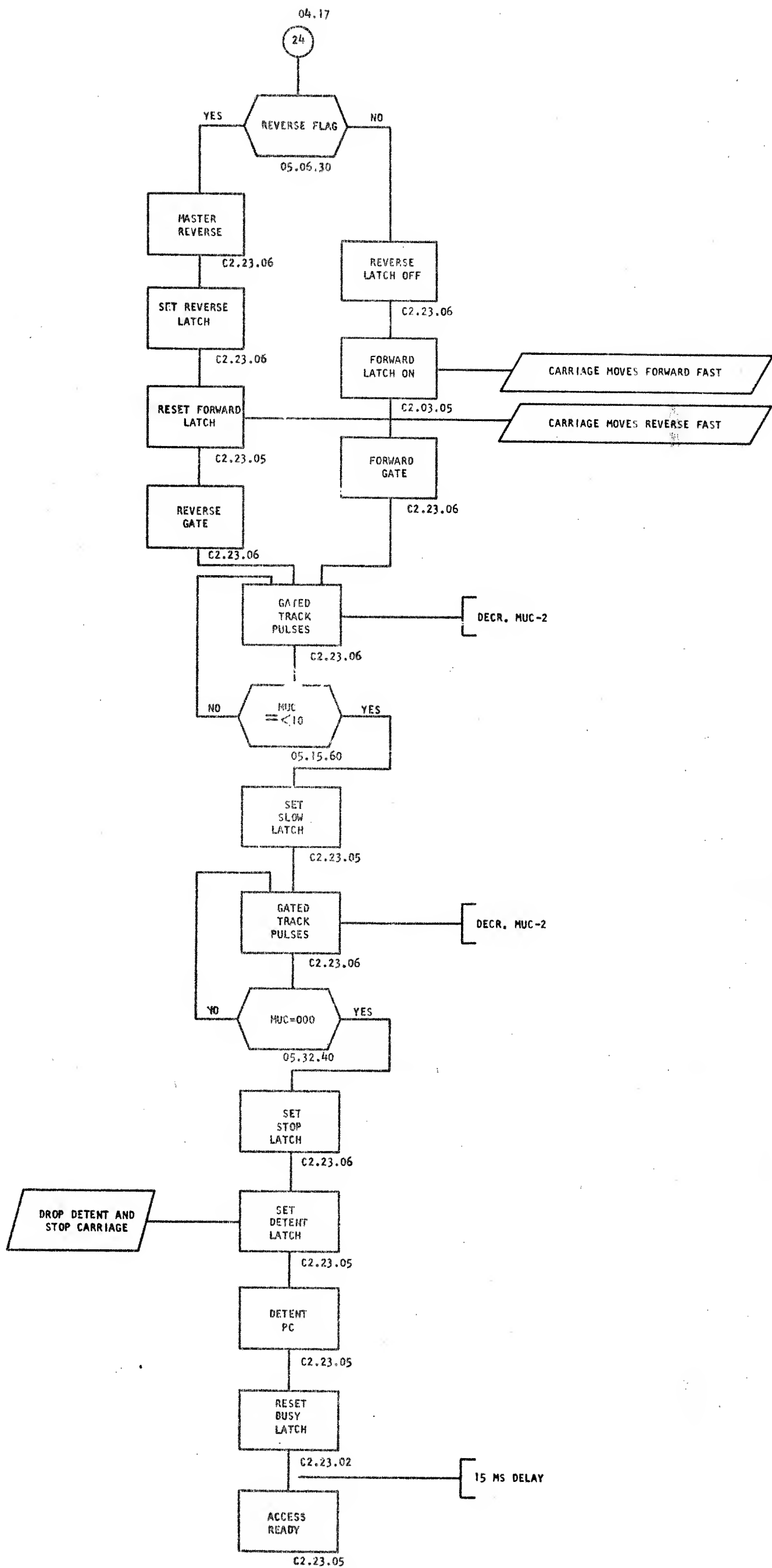


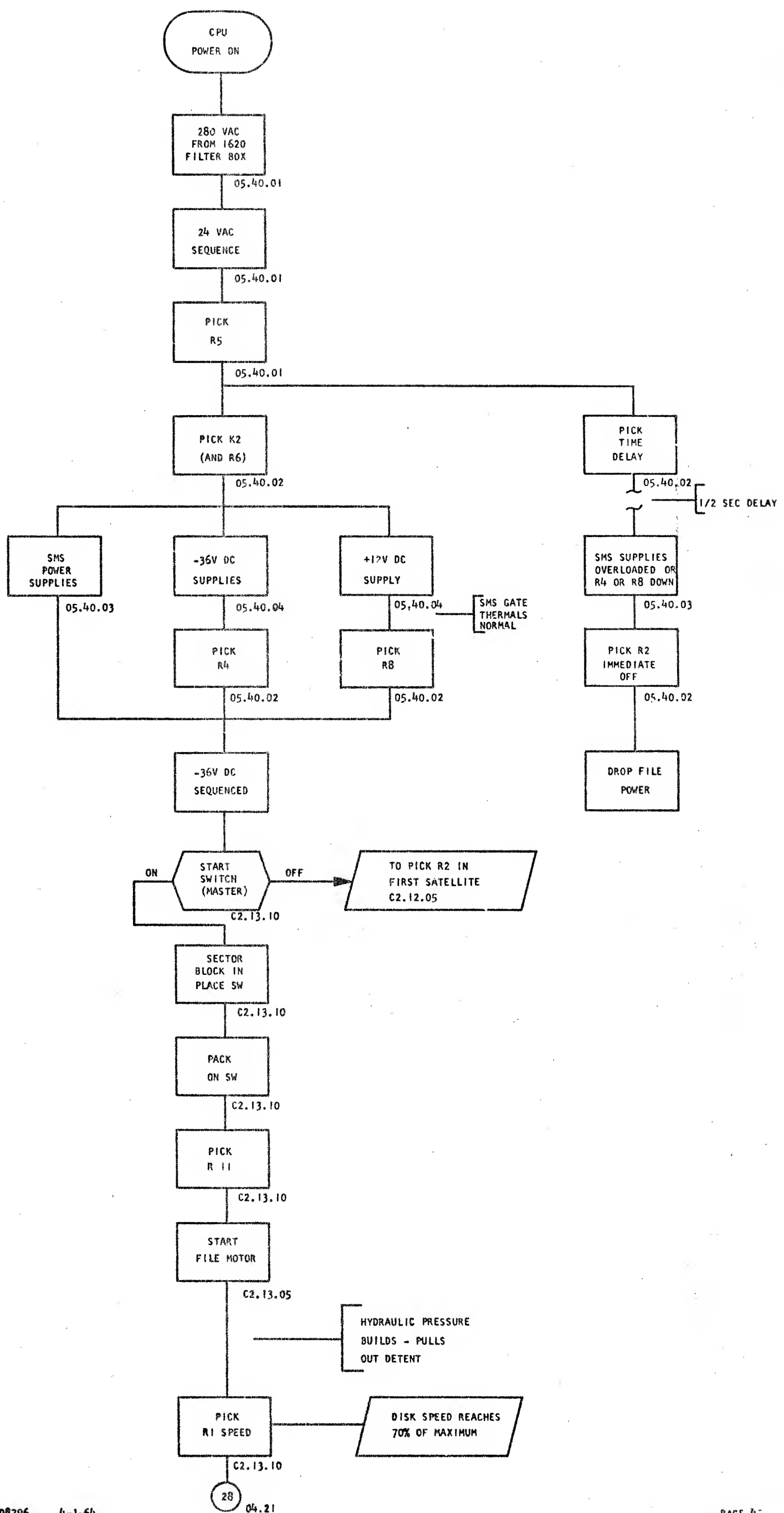


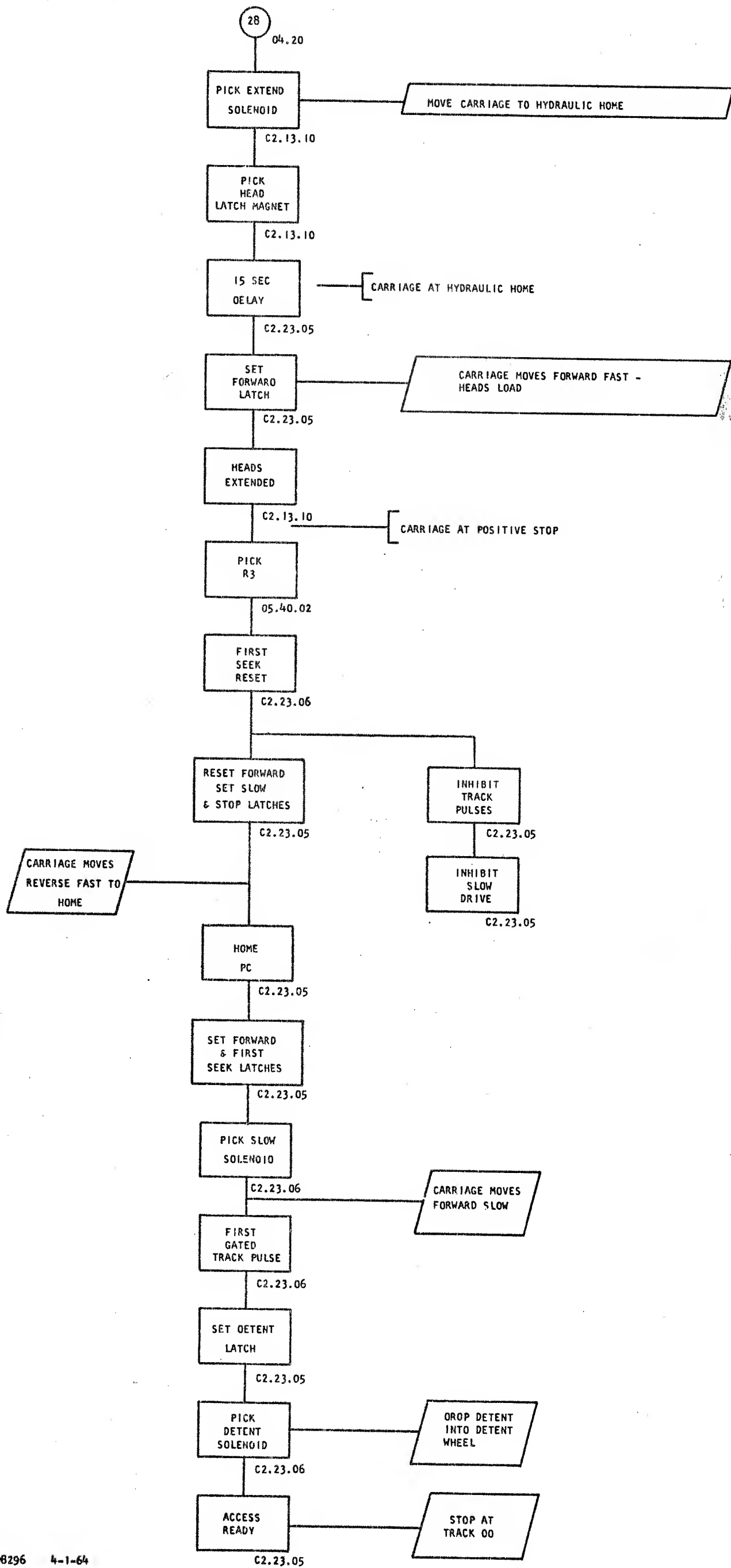






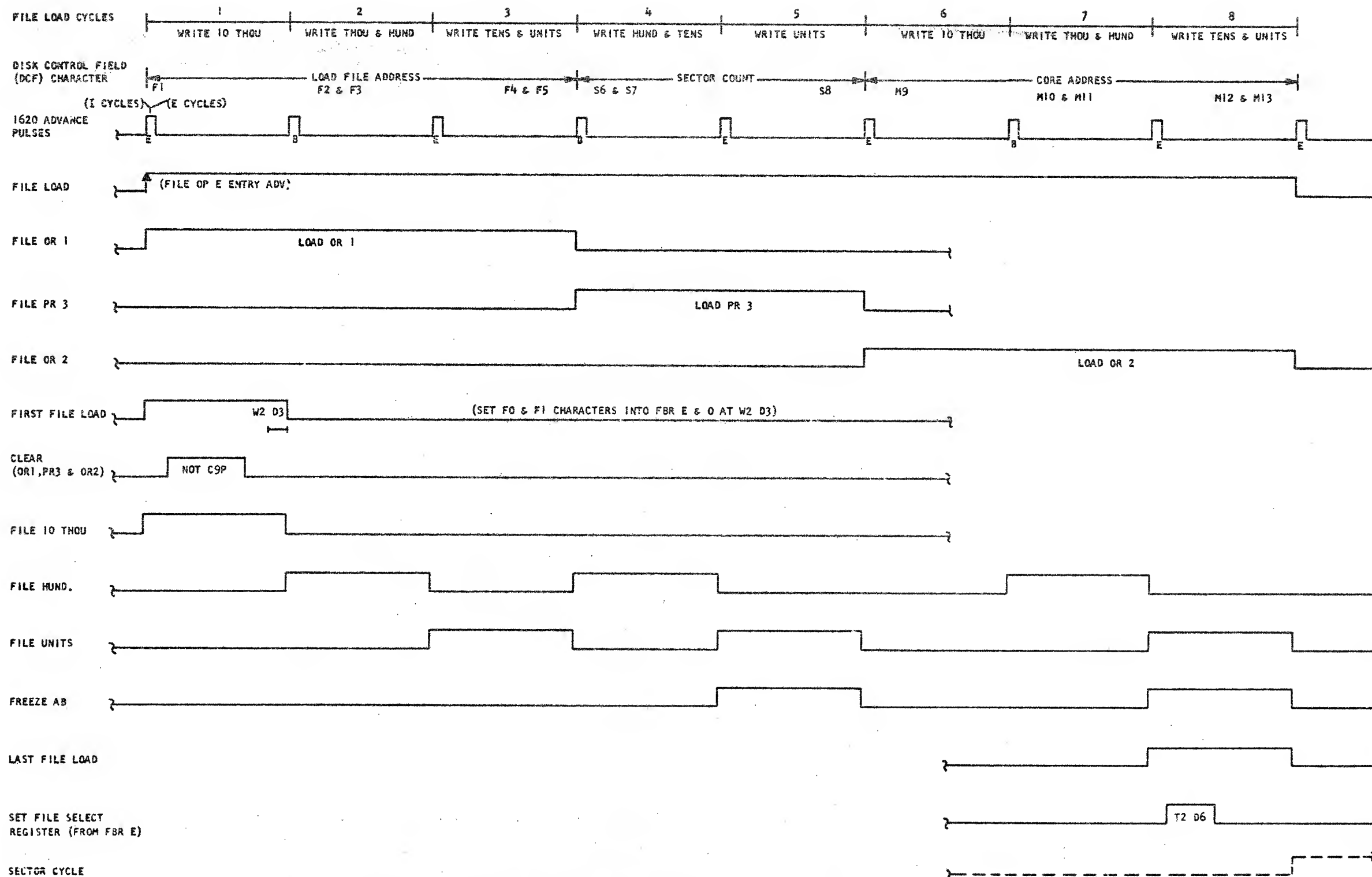






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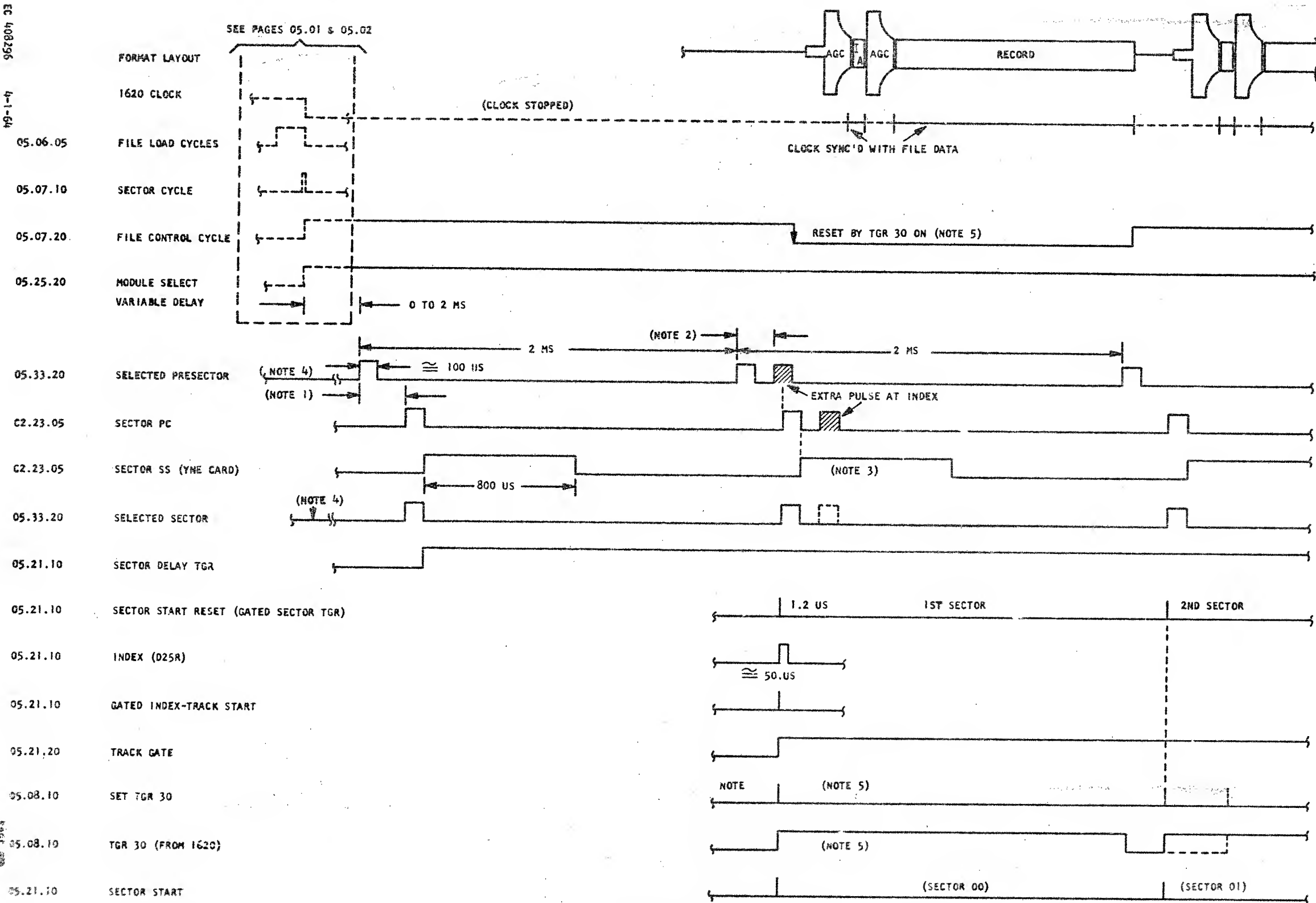
1620 CYCLES	
FILE LOAD CYCLES	05.01
SECTOR CYCLE, FILE CONTROL CYCLE	05.02
ADDRESS SEARCH CYCLES	
TRACK GATE & SECTOR START	05.03
READ 180 BIT PRE-ADDRESS AGC	05.04
SENSE GAPS	05.05
COMPARE I/A	05.06
DATA TRANSFER CYCLES	
READ 100 BIT PRE-RECORD AGC	05.07
READ RECORD	05.08
READ I/A WITHOUT COMPARE	05.14
READ & COMPARE I/A TO CORE DATA	05.15
READ & COMPARE RECORD	05.16
LATE CYCLE & WLR CHECK	05.09
WRITE 180 BIT PRE-ADDRESS AGC & GAP	05.12
WRITE INDELIBLE ADDRESS	05.13
WRITE 100 BIT PRE-RECORD AGC & GAP	05.10
WRITE RECORD	05.11
FILE SEEK CYCLES	
SEEK, MODE	05.17
SEEK, RETURN TO HOME	05.18
SEEK, DIRECT	05.19
POWER ON	
POWER ON & FILE MOTOR S. QUENCING	05.20
HEAD LOADING SEQUENCE	05.21



NOTES: 1. ABOVE TIMING FOR 1620-I OPERATION ONLY.

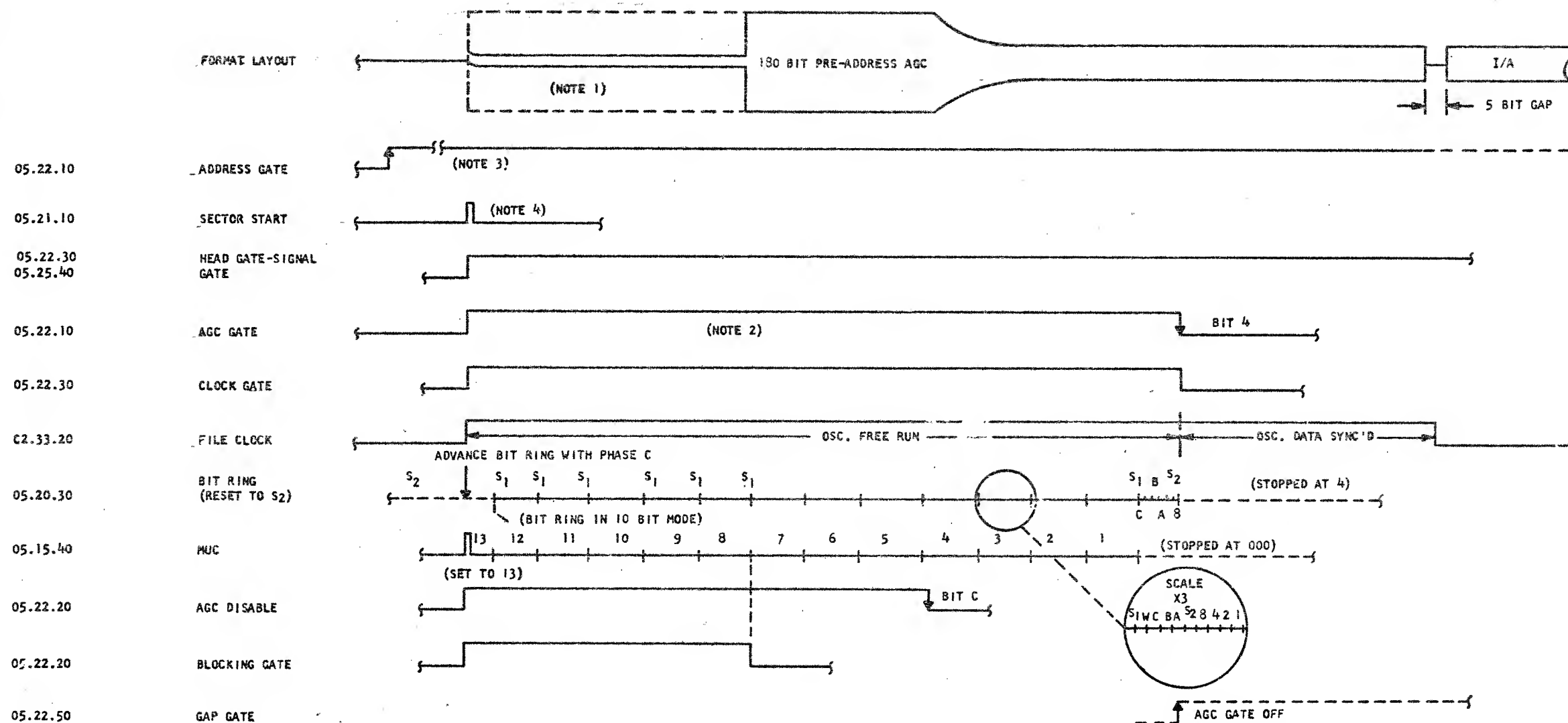


1. DASHED LINES SHOW END OF FILE OP. CAUSED BY FILE EXIT CONDITION.
2. SELECTED SECTOR (OR PRESECTOR) MAY ARRIVE ANY TIME AFTER MODULE SELECT IS CONDITIONED.
3. 1620 CLOCK STOPS AT W5 OF SECTOR CYCLE IF "FILE NOT READY" IS UP.
4. SEE PAGE 05.09 FOR LATE CYCLE TIMING.

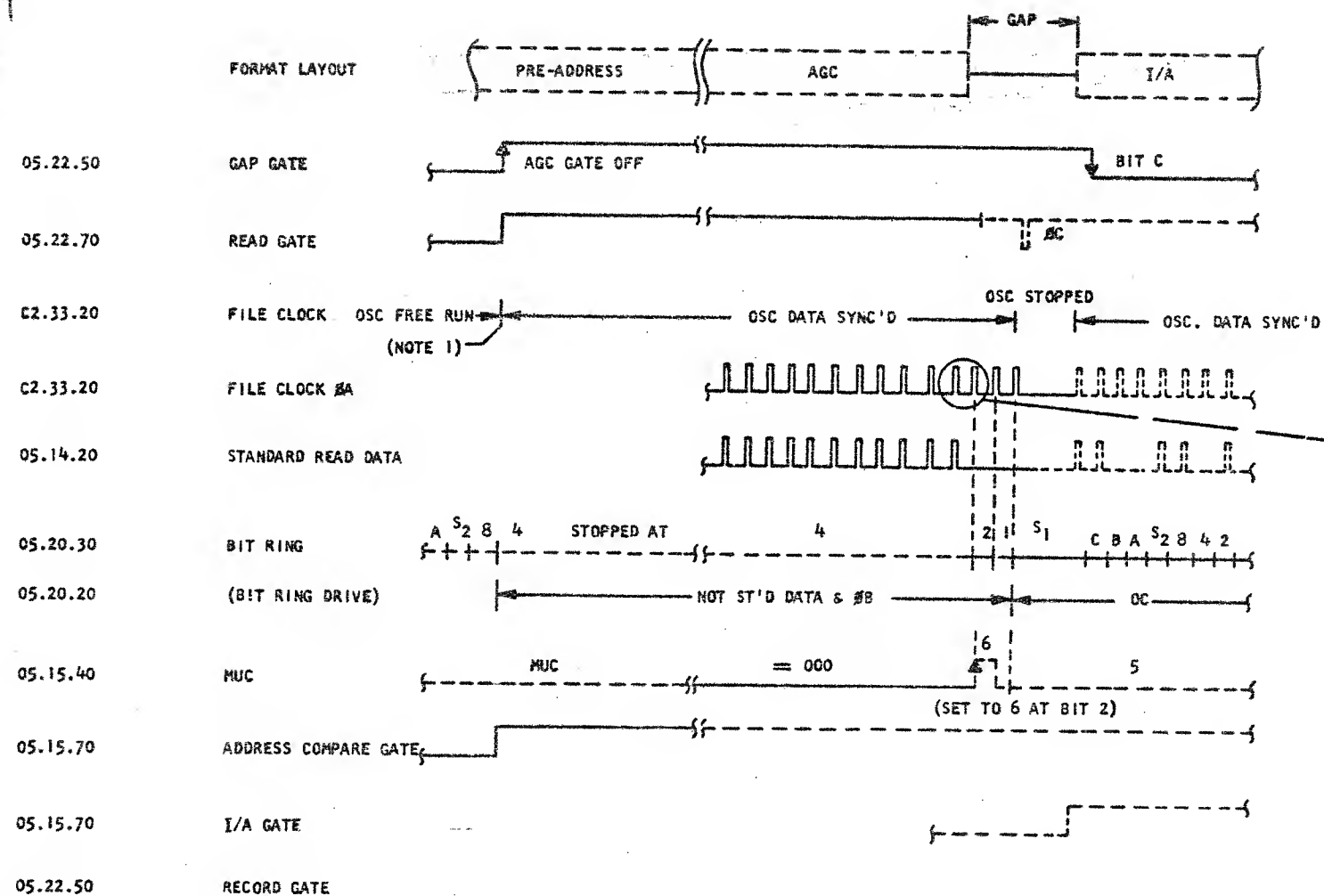


NOTES:

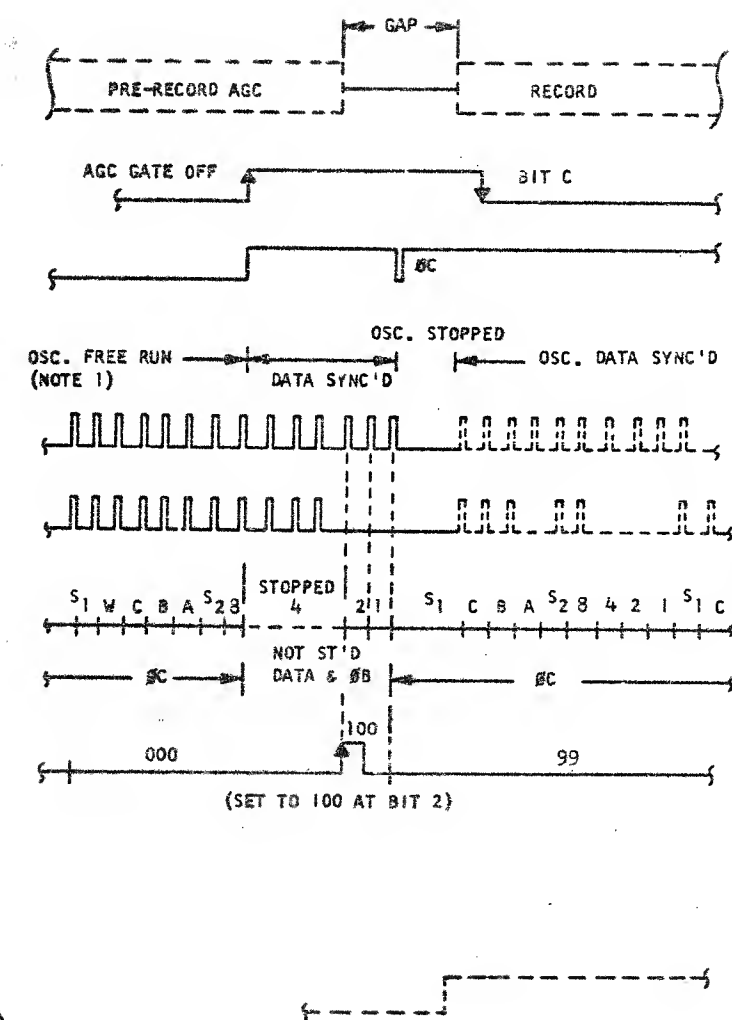
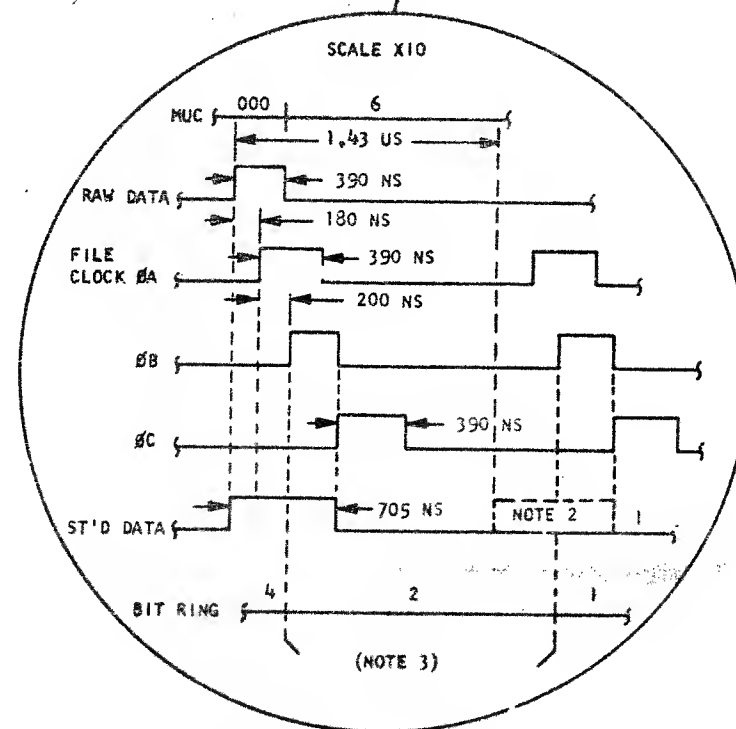
1. TIME FROM LEADING EDGE OF PRESECTOR TO LEADING EDGE OF SECTOR IS A FUNCTION OF DISTANCE BETWEEN P CELLS IN SECTOR BLOCK.
2. TIME BETWEEN LEADING EDGES OF THE TWO PRESECTOR (OR SECTOR) PULSES AT INDEX IS A FUNCTION OF THE DISTANCE BETWEEN THE TWO SLOTS IN TIMING DISK AT INDEX.
3. SECTOR SS BLOCKS ANY SECTOR PULSE FOLLOWING ANOTHER PULSE WITHIN 800 US.
4. SELECTED SECTOR OR PRESECTOR MAY ARRIVE ANY TIME AFTER MODULE SELECT COMES UP.
5. SHOWN IN TRACK OP. (DASHED LINE SHOWS SECTOR OP).

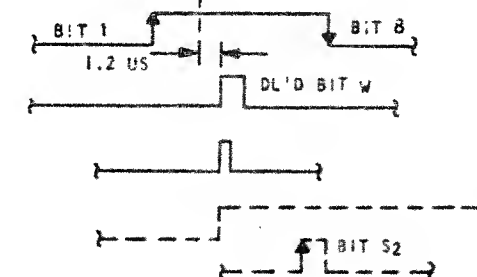


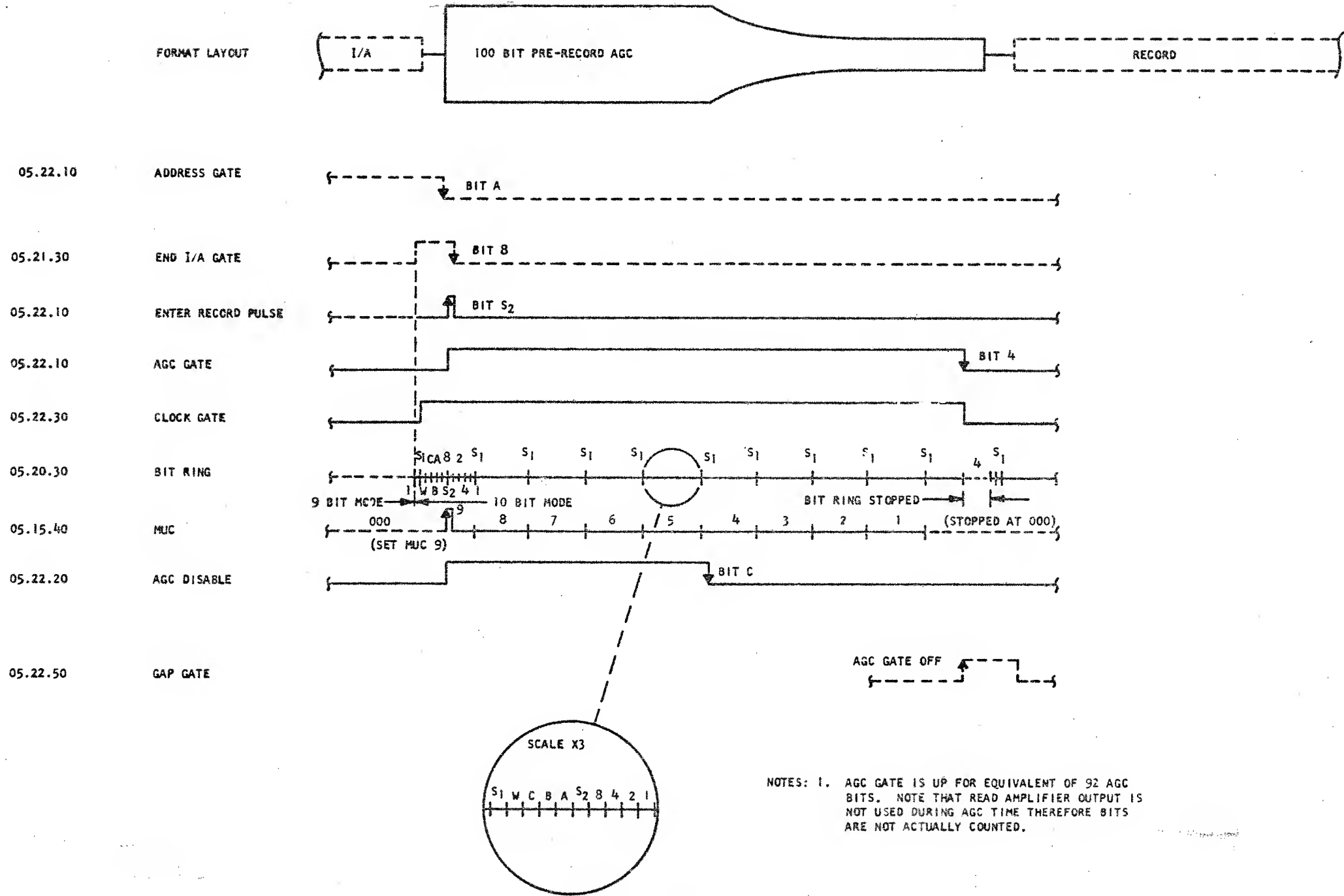
- NOTES:
1. DOTTED LINE SHOWS EFFECT OF BLOCKING GATE ON READ AMPLIFIER OUTPUT.
 2. AGC GATE UP FOR EQUIVALENT OF 132 AGC BITS. NOTE THAT READ AMPLIFIER OUTPUT IS NOT USED DURING AGC TIME THEREFORE BITS ARE NOT ACTUALLY COUNTED.
 3. ADDRESS GATE IS SET BY FILE RESET ON FIRST SECTOR, AND BY FUNCTIONAL RESET ON SUBSEQUENT SECTORS OF OPERATION.
 4. ON FULL TRACK OPS, TGR 30 IS SET AT SECTOR START. ON RBC FULL TRACK & WRITE FULL TRACK EARLY WRITE IS ALSO SET. SEE PAGE 05.10 FOR OTHER DETAILS OF EARLY WRITE CYCLE.

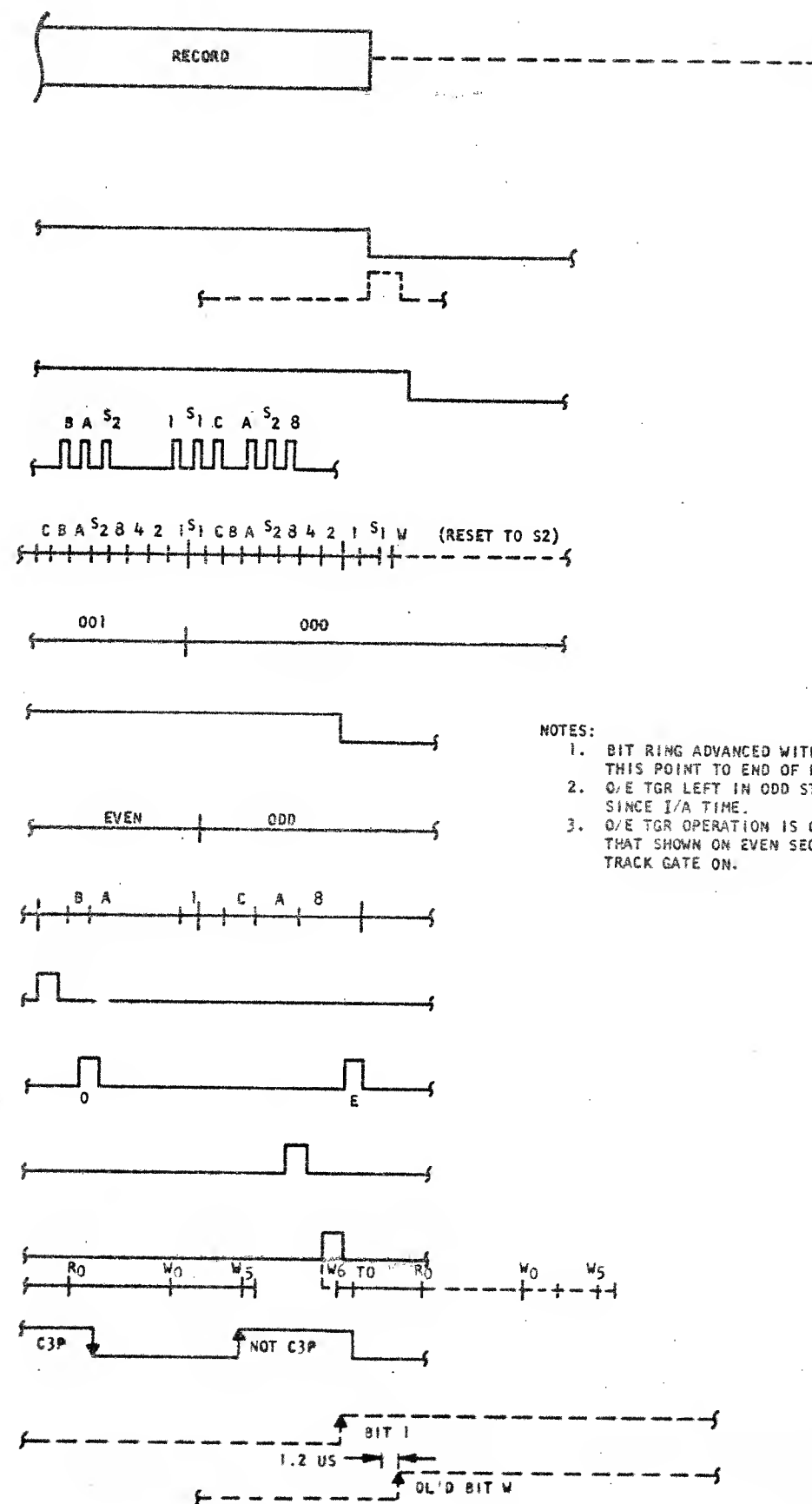
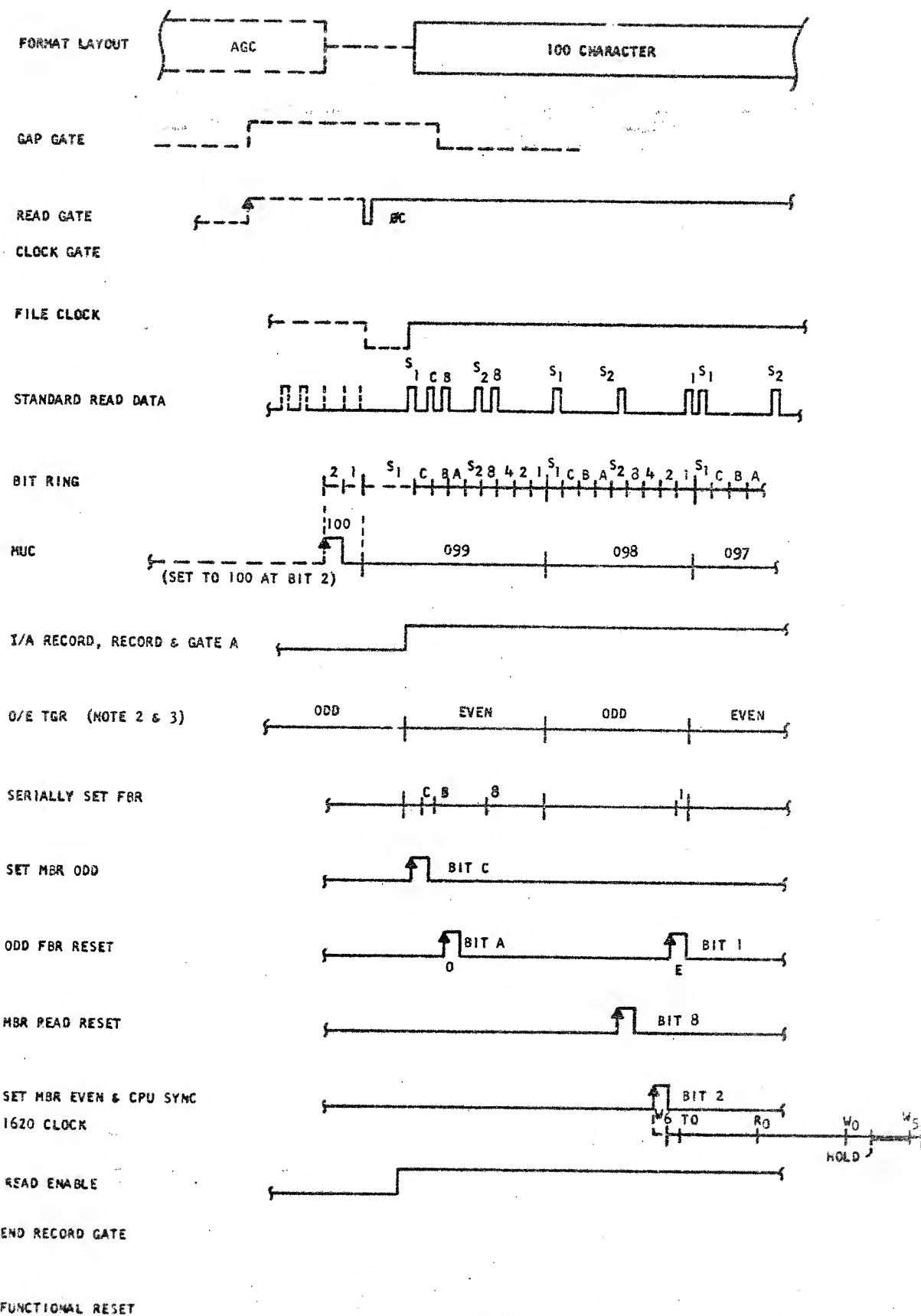


- NOTES:
1. OSCILLATOR OUTPUT WILL JITTER HERE.
 2. NOT STANDARD DATA
 3. BIT RING NORMALLY ADVANCED AT RISE OF ϕC :
BIT RING ADVANCED AT RISE OF ϕB DURING GAP SENSE ONLY.







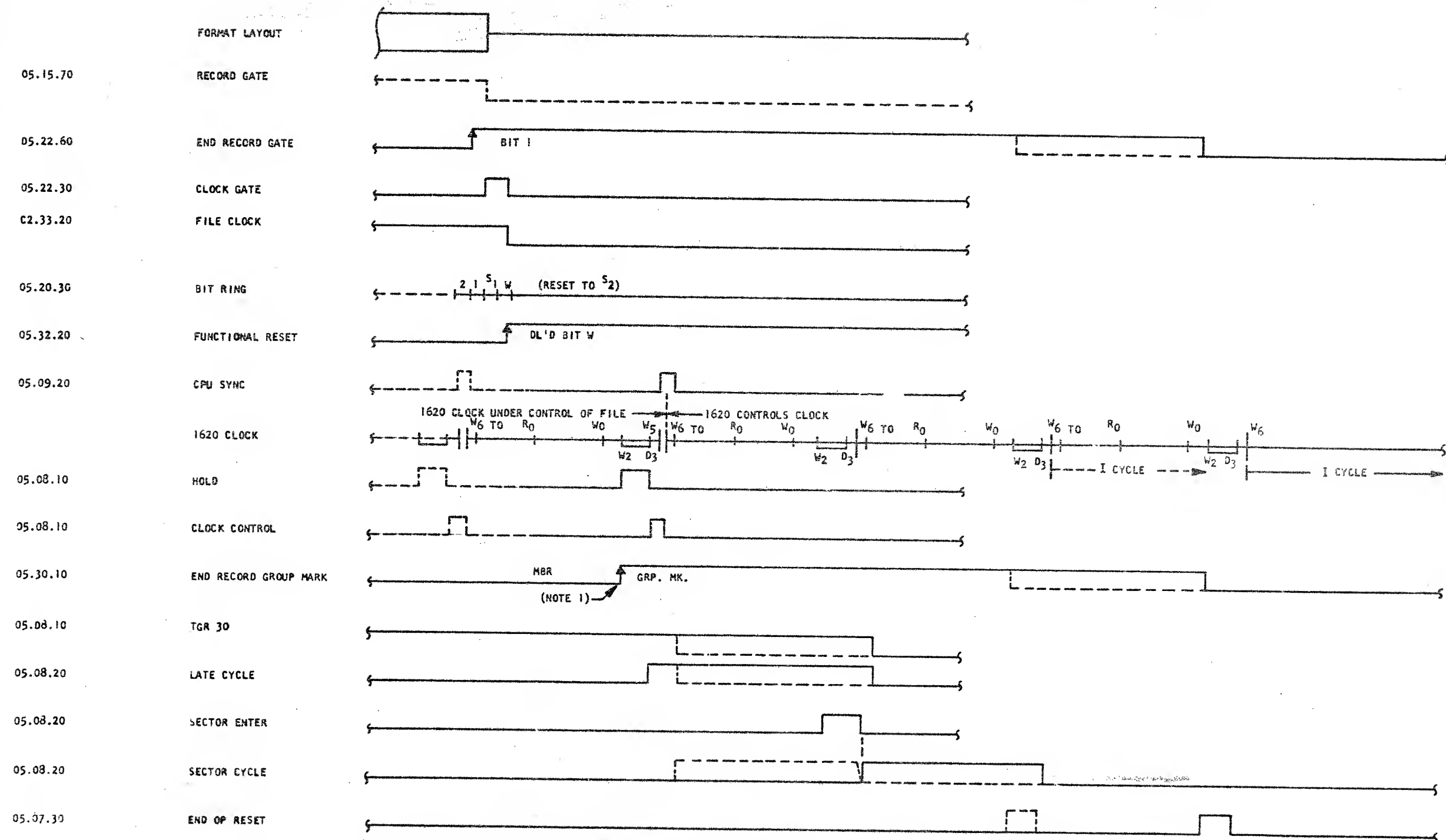


NOTES:

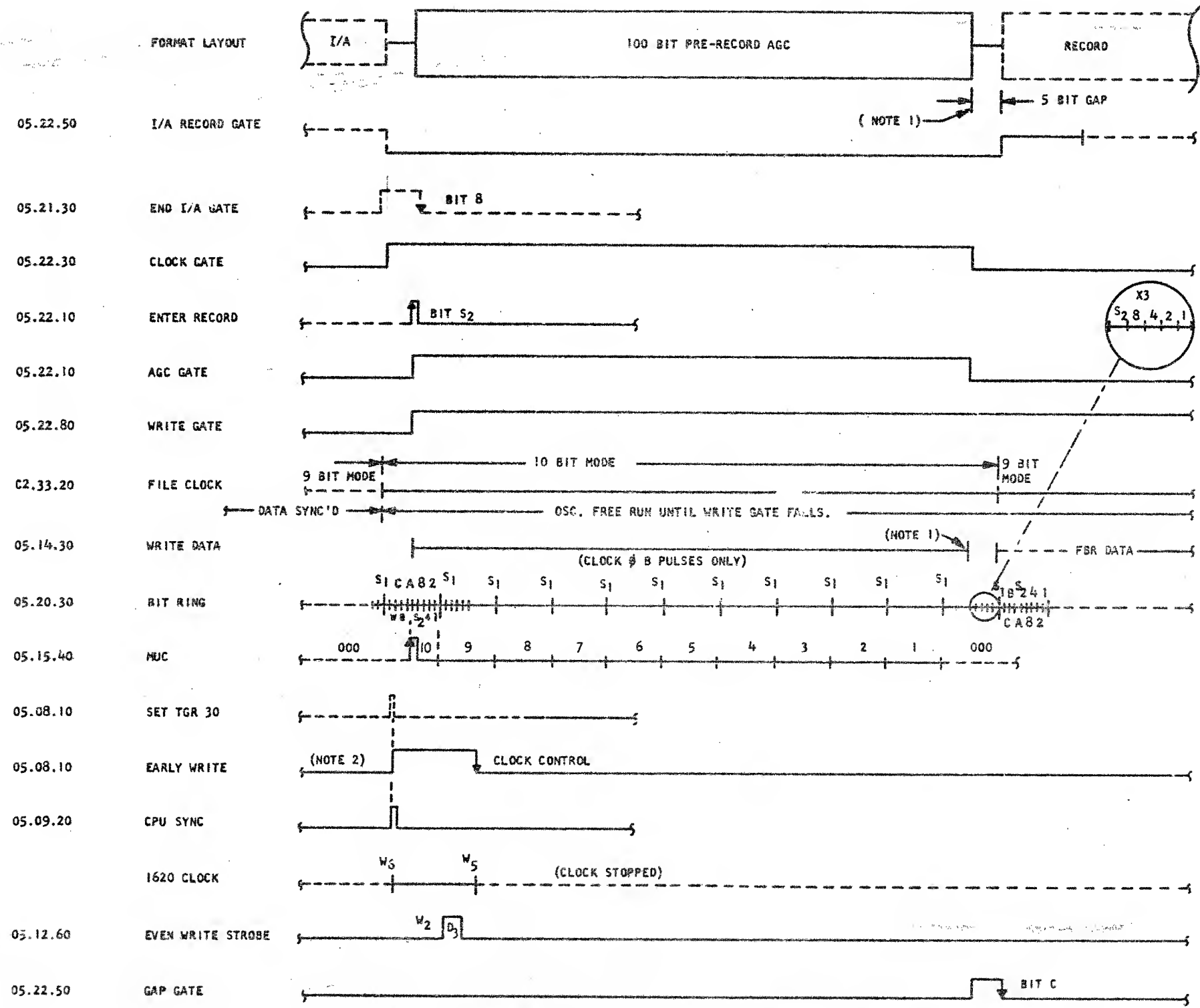
1. BIT RING ADVANCED WITH OC FROM THIS POINT TO END OF RECORD.
2. O/E TGR LEFT IN ODD STATUS SINCE I/A TIME.
3. O/E TGR OPERATION IS OPPOSITE THAT SHOWN ON EVEN SECTORS WITH TRACK GATE ON.

LATE CYCLE & WLR CHECK

05.09



- NOTES: 1. SET WLR ERROR IF NO GROUP MARK ON A WLR OP.
2. SOLID LINES SHOW WLR OP. NOTE THAT THE OPERATION IS SHORTENED BY ONE 1620 CLOCK CYCLE ON NO WLR OP.
3. SEE PAGE 05.02 FOR FILE EXIT TIMING..



NOTES: 1. ABSENCE OF WRITE DATA CAUSES 5 BIT GAP.
2. EARLY WRITE LOADS FIRST 2 CHARACTERS INTO MBR EVEN, THEN TRANSFERS MBR EVEN TO FBR EVEN. SEE 'WRITE RECORD' 05.11

05.22.50

GAP GATE

05.22.80

WRITE GATE

02.33.20

FILE CLOCK

05.20.30

BIT RING

05.15.40

MJC

05.22.50

I/A RECORD, RECORD & GATE A

05.08.30

05.12.70

O/E TGR & GATE OUT FBR SERIAL (NOTE 2)

05.09.30

GATE MBR (TO FBR)

05.12.50

FBR RESETS

05.12.60

ODD WRITE STROBE & CPU SYNC

05.12.60

EVEN WRITE STROBE

05.09.20

1620 CLOCK

05.09.10

WRITE ENABLE

05.12.70

SERIAL FBR DATA

05.14.30

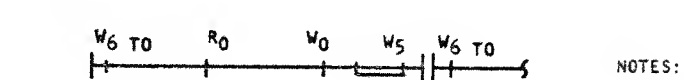
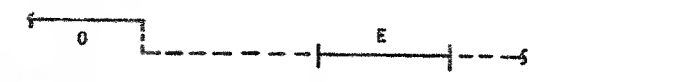
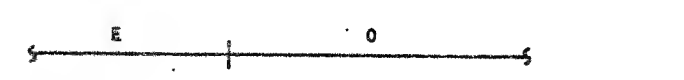
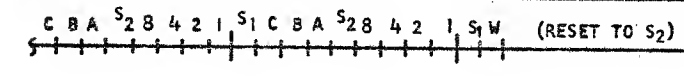
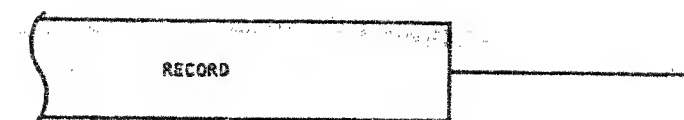
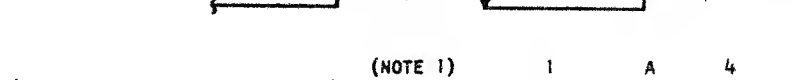
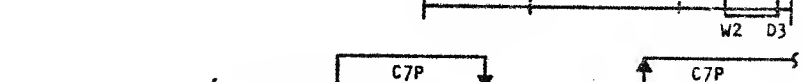
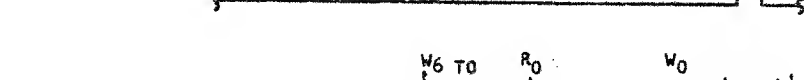
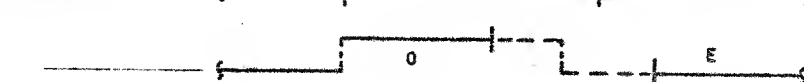
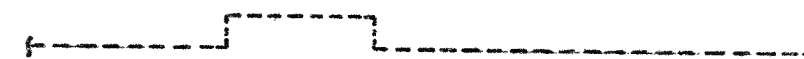
WRITE DATA (08)

05.22.60

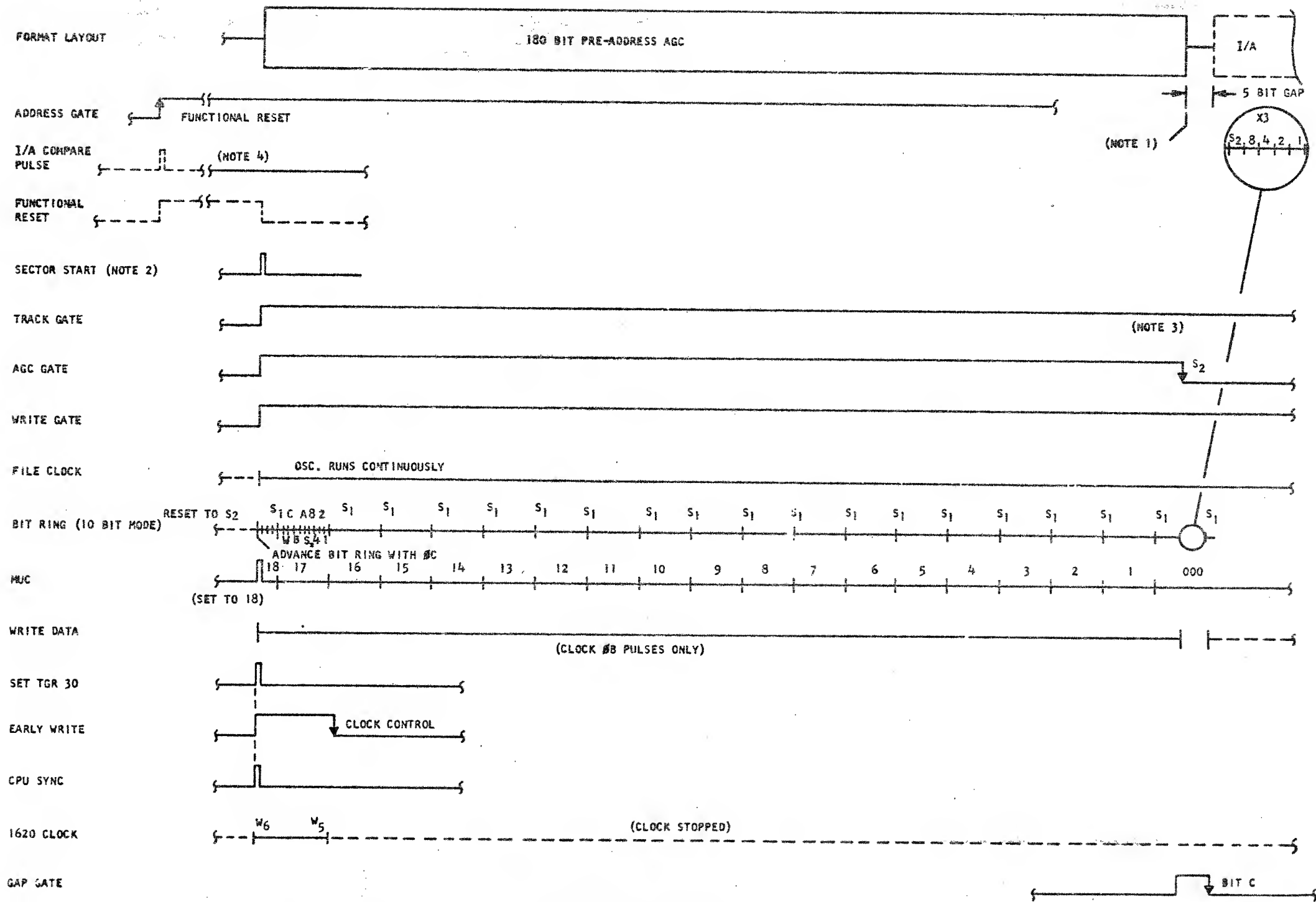
END RECORD GATE

05.32.20

FUNCTIONAL RESET



NOTES:
1. SEE 05.10 FOR EARLY CYCLE OP
2. O/E TGR OPERATION IS OPPOSITE THAT SHOWN ON EVEN SECTORS WITH TRACK GATE ON.

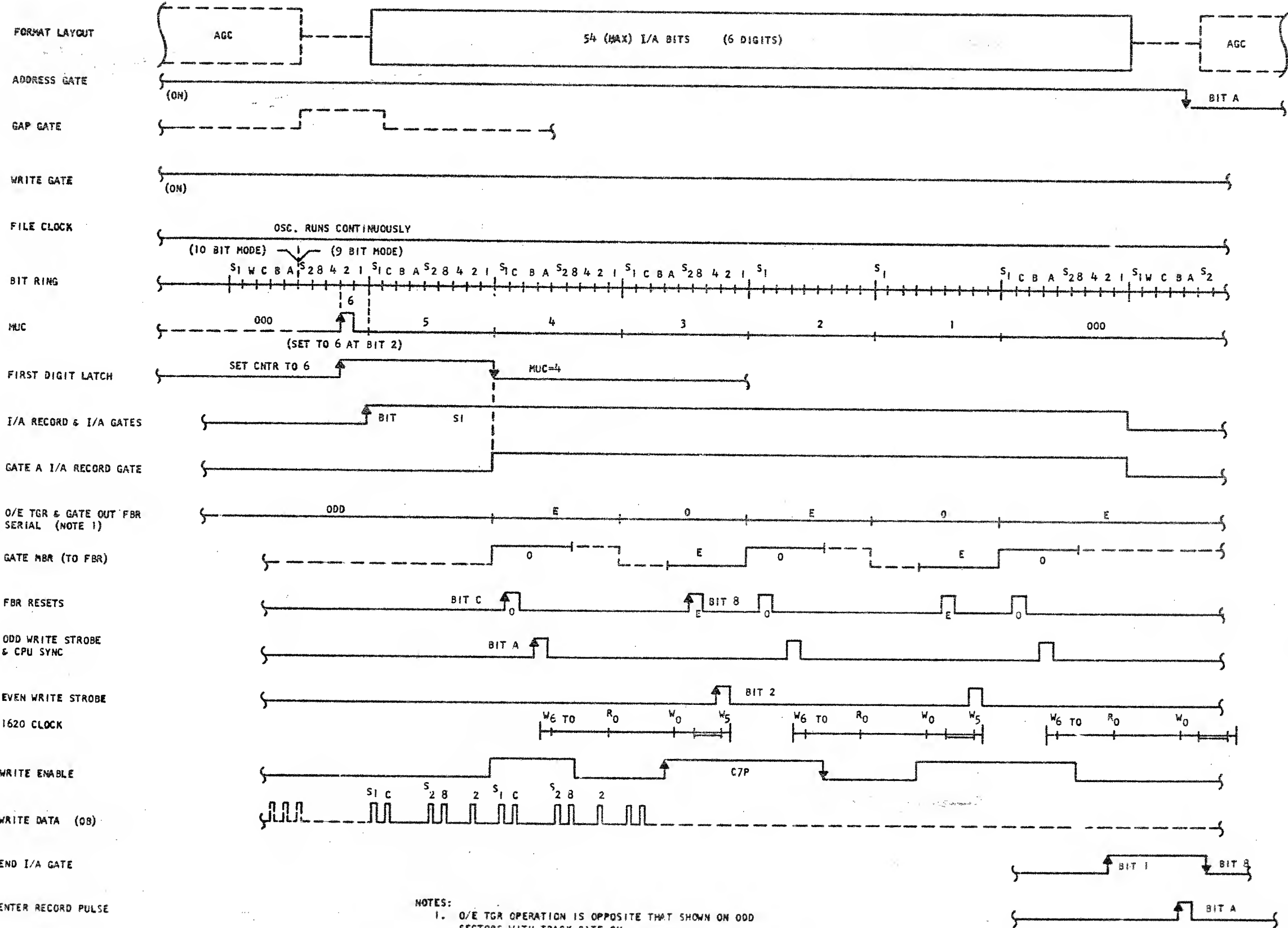


- NOTES:
1. ABSENCE OF WRITE DATA CAUSES 5 BIT GAP
 2. ALSO, GATED INDEX IF FIRST SECTOR OF TRACK OP.
 3. RESET AT END OP.
 4. SUCCESSFUL ADDRESS COMPARE PRECEDED THIS OP.

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PAGE 60



NOTES:

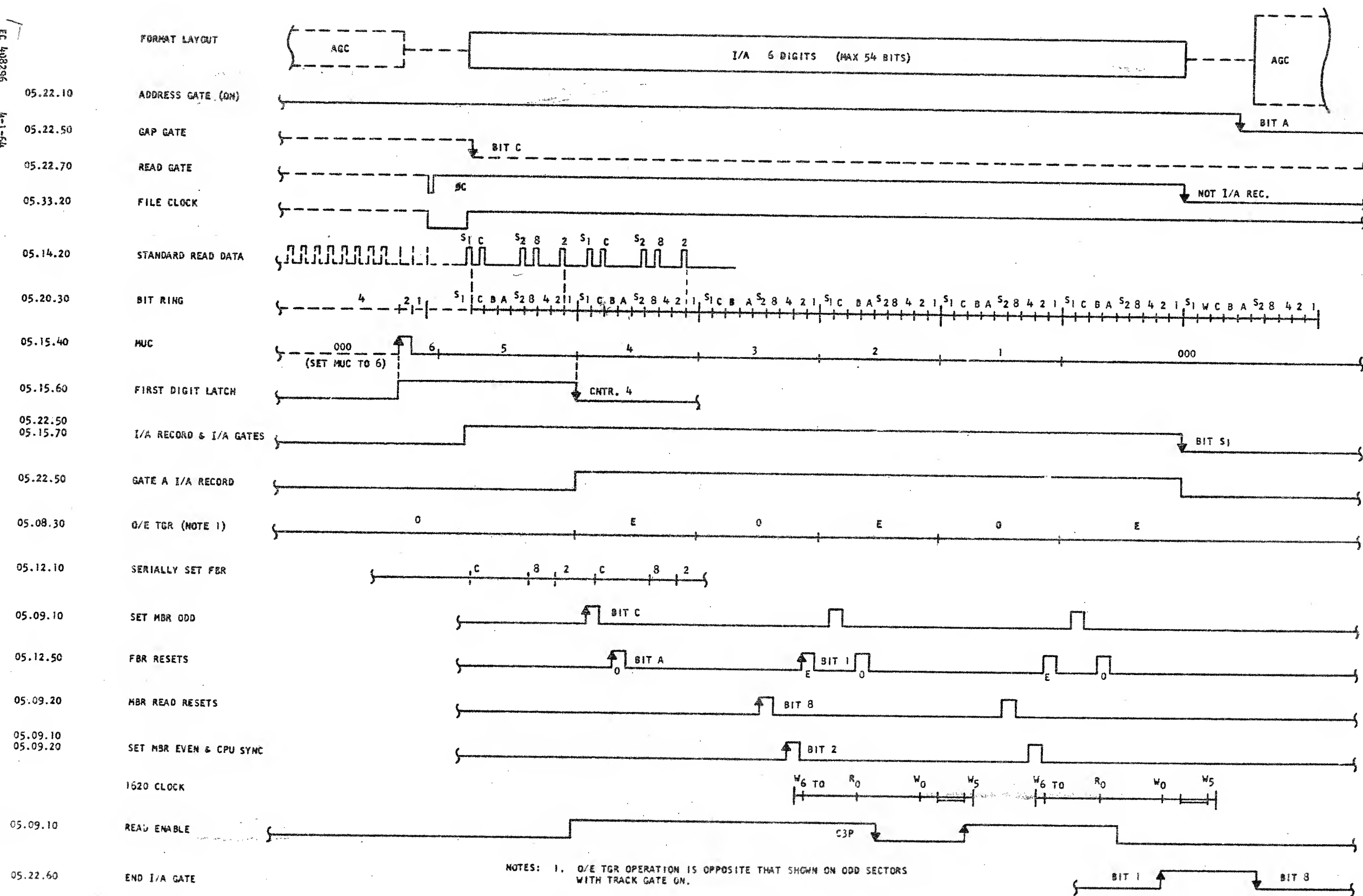
1. O/E TGR OPERATION IS OPPOSITE THAT SHOWN ON ODD SECTORS WITH TRACK GATE ON.

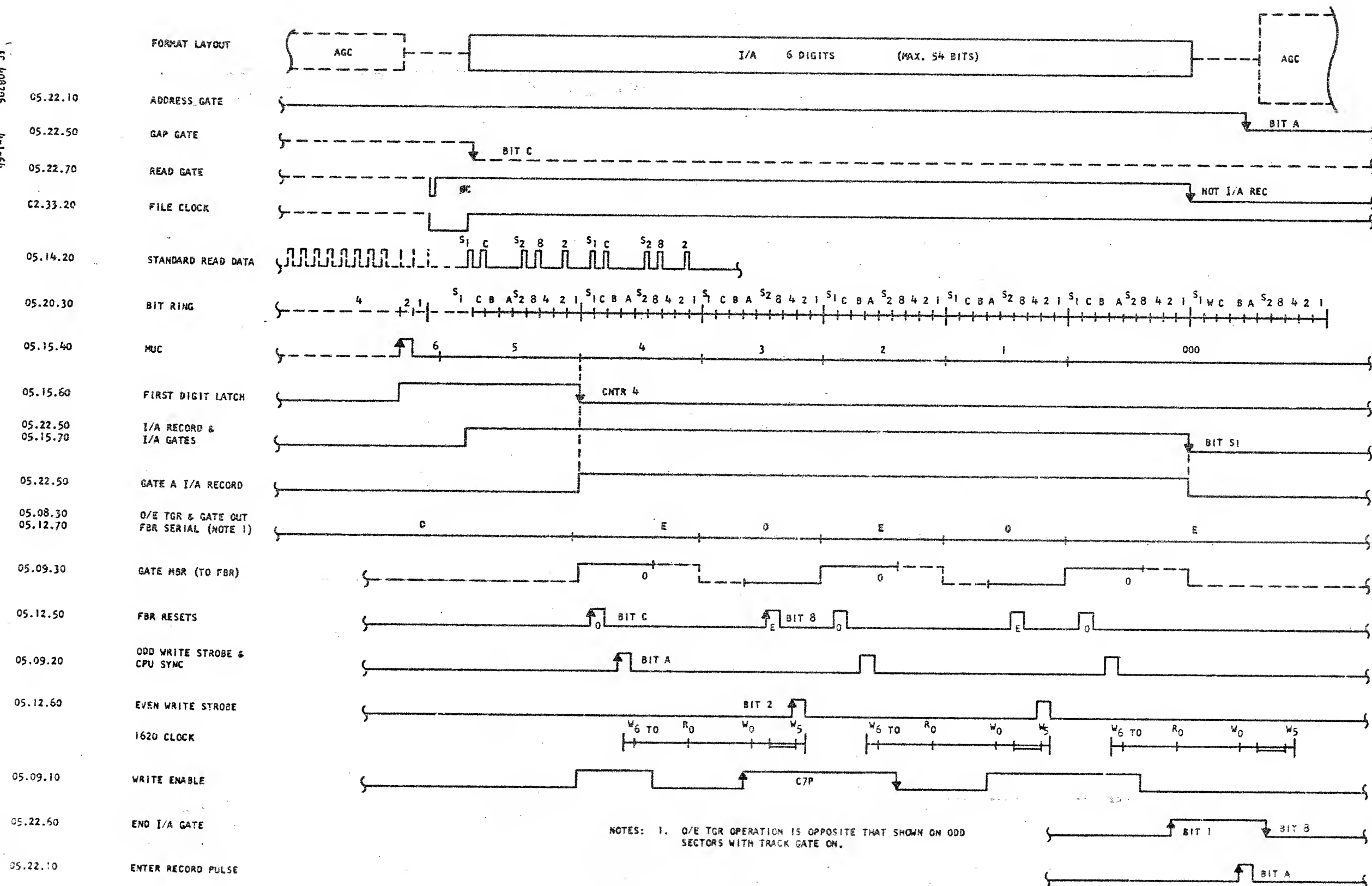
2. SEE 05.12 FOR EARLY WRITE CYCLE OPERATION.

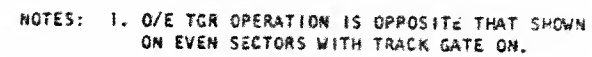
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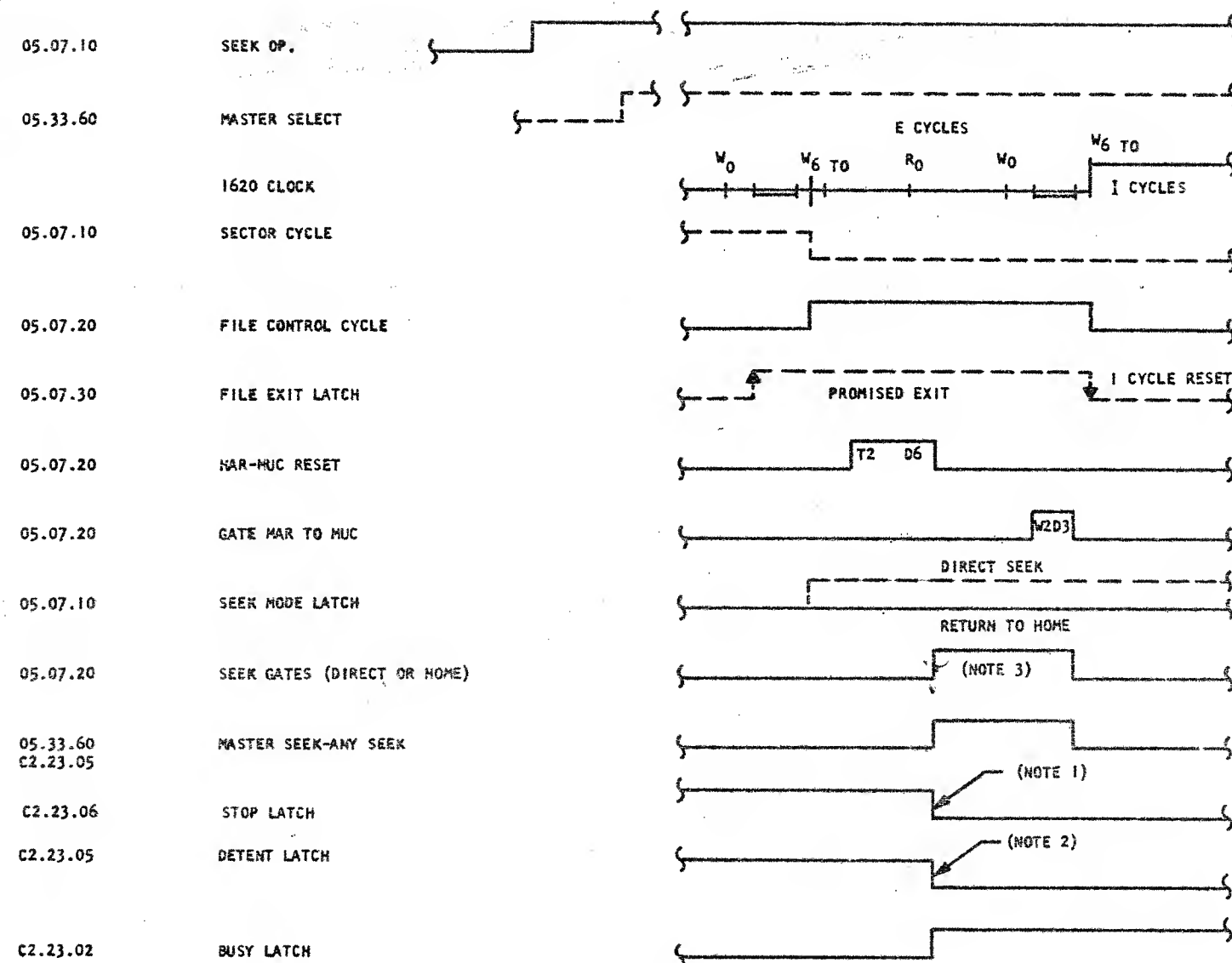
WRITE INDELIBILE ADDRESS

05.13





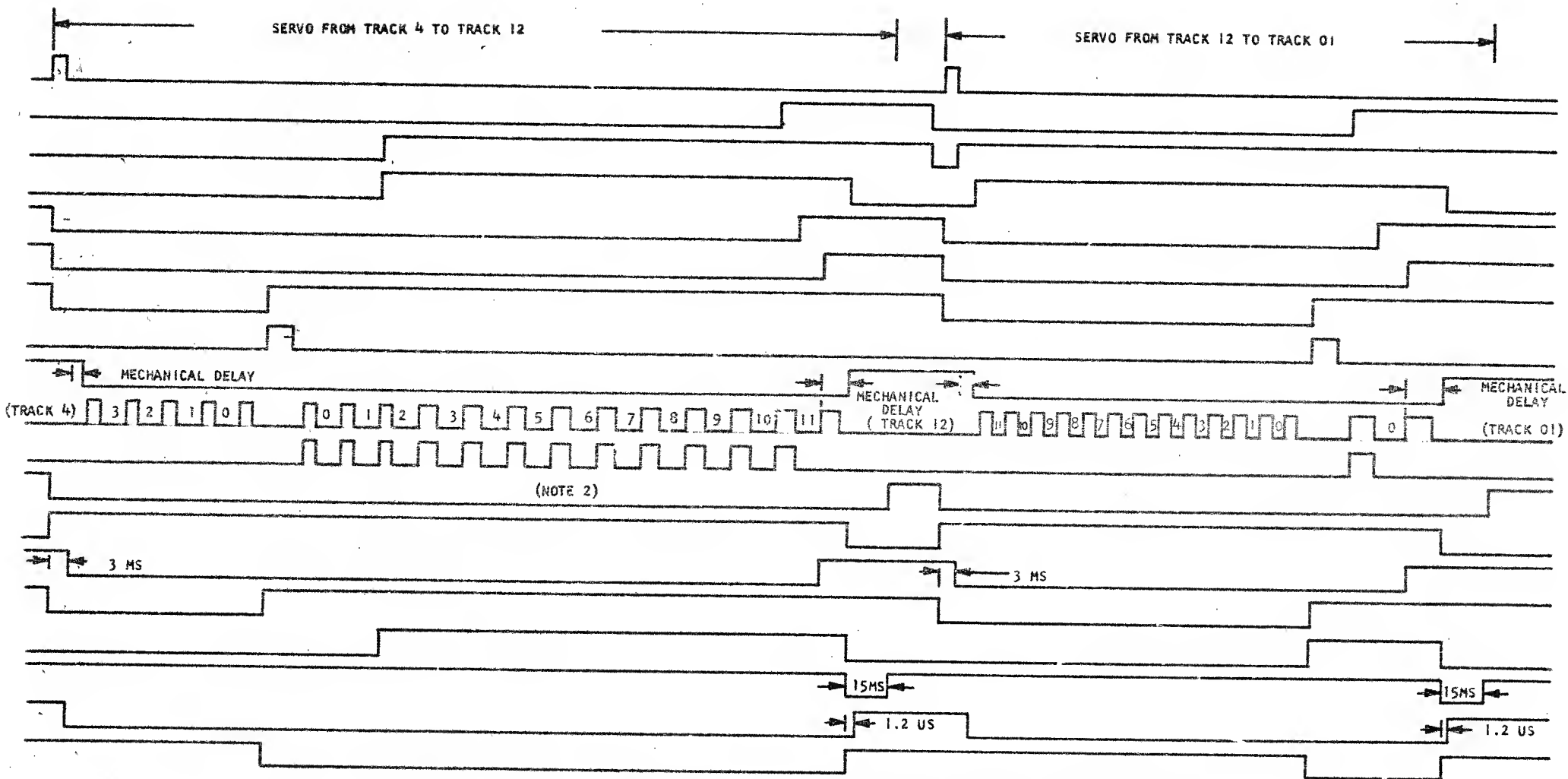




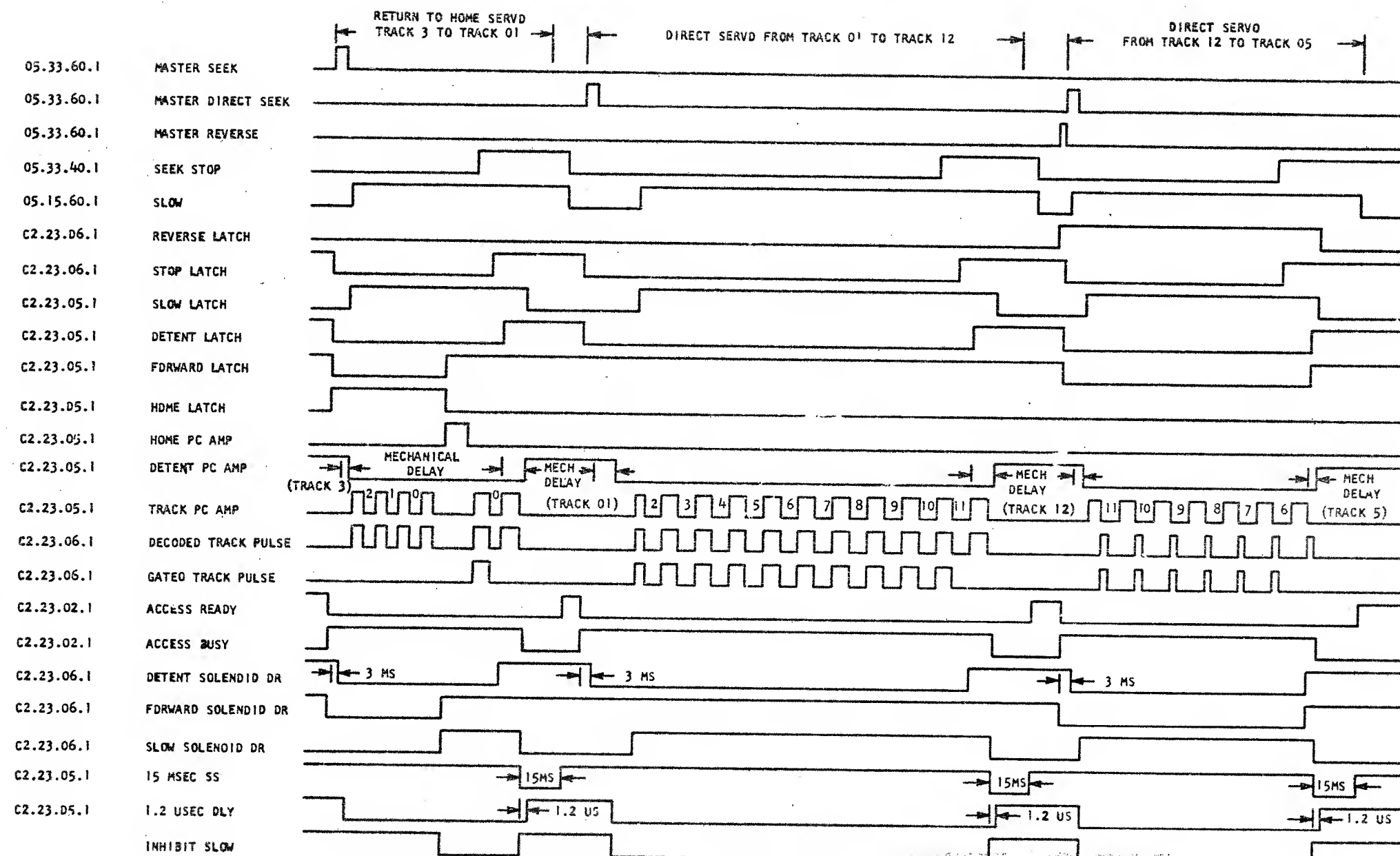
NOTES:

1. CONDITION TRACK PULSE GATE AND DETENT LATCH SET GATE.
2. START TO PULL OUT DETENT
3. BLOCKS THE STEPPING OF MUC

05.33.60.1 MASTER SEEK
05.33.40.1 SEEK STOP
05.15.60.1 SLOW
C2.23.05.1 SLOW LATCH
C2.23.06.1 STOP LATCH
C2.23.05.1 DETENT LATCH
C2.23.05.1 FORWARD LATCH
C2.23.05.1 HOME P.C. —
C2.23.05.1 DETENT P.C. —
C2.23.05.1 TRACK PULSE P.C.
C2.23.06.1 GATED TRACK PULSE
C2.23.02.1 ACCESS READY
C2.23.02.1 ACCESS BUSY
C2.23.06.1 DETENT SOL DRIVER
C2.23.06.1 FORWARD SOL DRIVER
C2.23.06.1 SLOW SOL DRIVER
C2.23.05.1 15 M SEC SINGLE SHOT
C2.23.05.1 1.2 USEC DLY
C2.23.05.1 INHIBIT SLOW

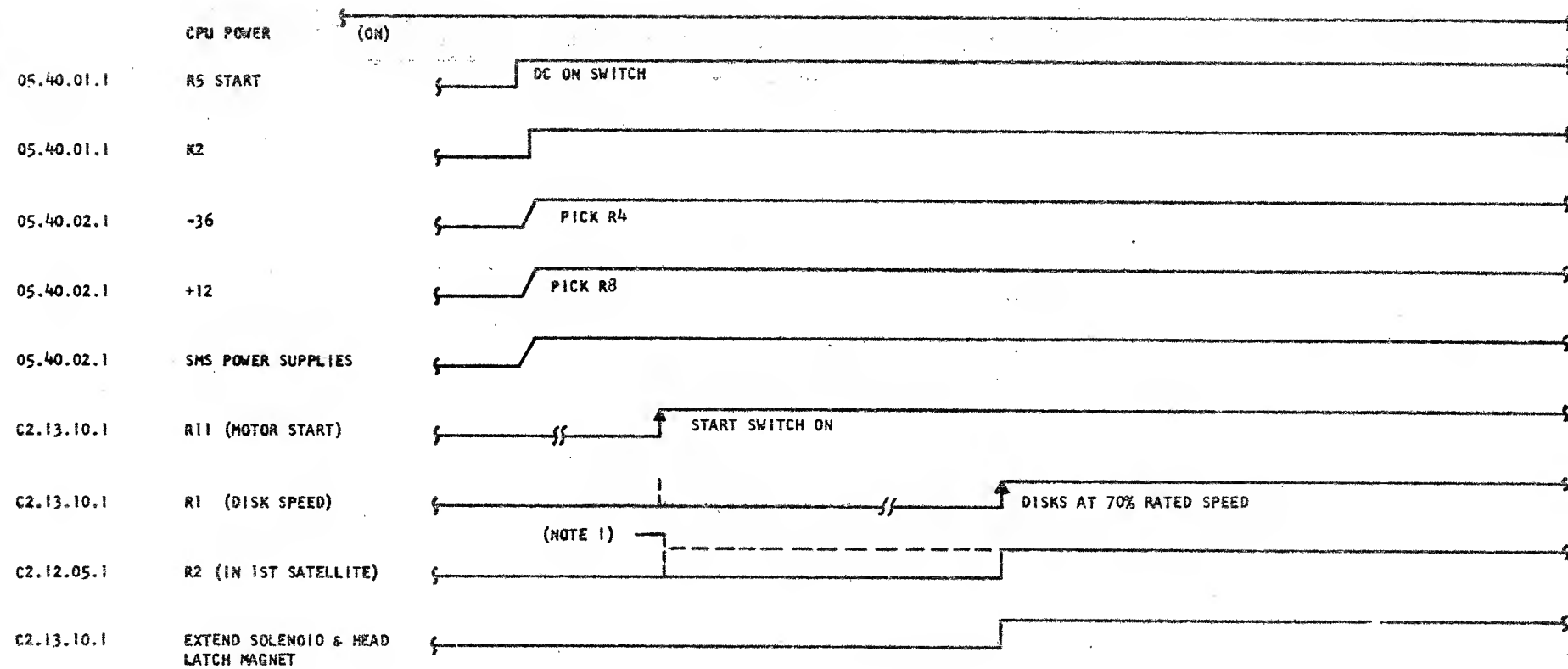


NOTES: 1. NUMBERS BESIDE TRACK PULSES CORRESPOND TO TRACK LOCATION.
2. SMALLER WIDTH TRACK PULSES ON LEFT ARE CAUSED BY HIGHER CARRIAGE SPEED



NOTE:

1. NUMBERS BESIDE TRACK PULSES CORRESPOND TO TRACK LOCATION..

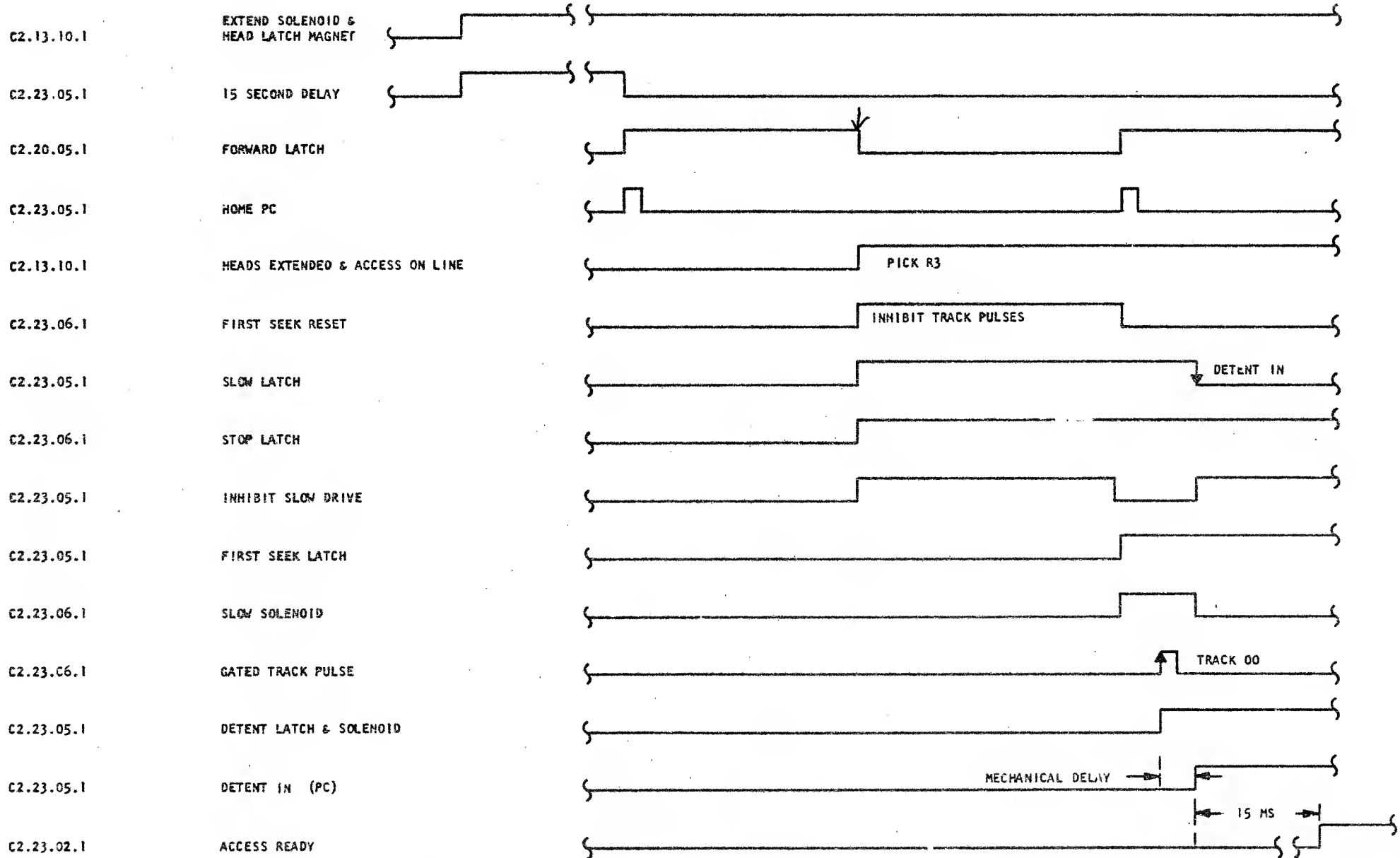


NOTES:

1. R2 PICKS HERE IF MASTER START SWITCH OFF
2. FOR DETAILED POWER ON-OFF TIMINGS. SEE LOGIC PAGE 05.40.09.1

EC 408296

4-1-64



INDEX

HOW TO READ THE SYMBOLS	06.01
BIT RING	06.04
CLOCK, FILE	06.07
ERROR CIRCUITS, FILE	06.08
HEAD ADDRESS REGISTER (HAR)	06.03
MULTIPLE USE COUNTER (MUC)	06.05
READ AMPLIFIER	06.06
RESETS, FILE	06.09
SELECT REGISTER, FILE	06.02

1. LOGIC BLOCK DESIGNATIONS

(A) AND



(B) OR



(C) INVERTER



(D) AMPLIFIER



(E) SINGLE SHOT



(F) TIME DELAY



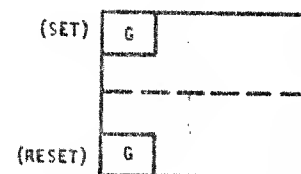
(G) FLIP LATCH



(H) FLIP FLOP (TRIGGER)



(I) GATE

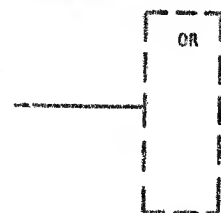


(J) OSCILLATOR



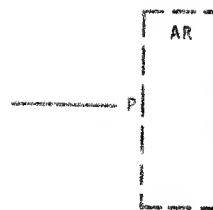
2. SIGNAL LINE DESIGNATIONS

(A)



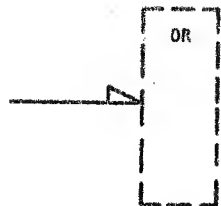
THE MORE POSITIVE LEVEL SATISFIES THE INDICATED FUNCTION.

(C)



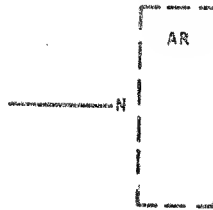
A POSITIVE (AC) SHIFT ACTIVATES THE CIRCUIT.

(B)



THE MORE NEGATIVE LEVEL SATISFIES THE INDICATED FUNCTION.

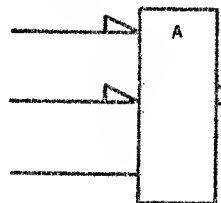
(D)



A NEGATIVE (AC) SHIFT ACTIVATES THE CIRCUIT.

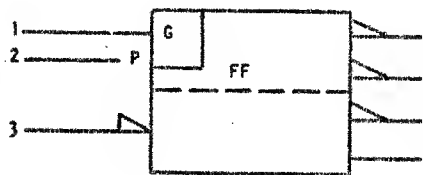
3. EXAMPLE APPLICATIONS

(A)



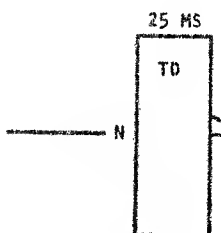
THE INDICATED FUNCTION IS SATISFIED WHEN THE INPUTS ASSUME THEIR INDICATED POLARITIES. AT THIS TIME, THE OUTPUTS ASSUME THEIR INDICATED POLARITIES (i.e. -AND-AND + IN: -OUT)

(B)

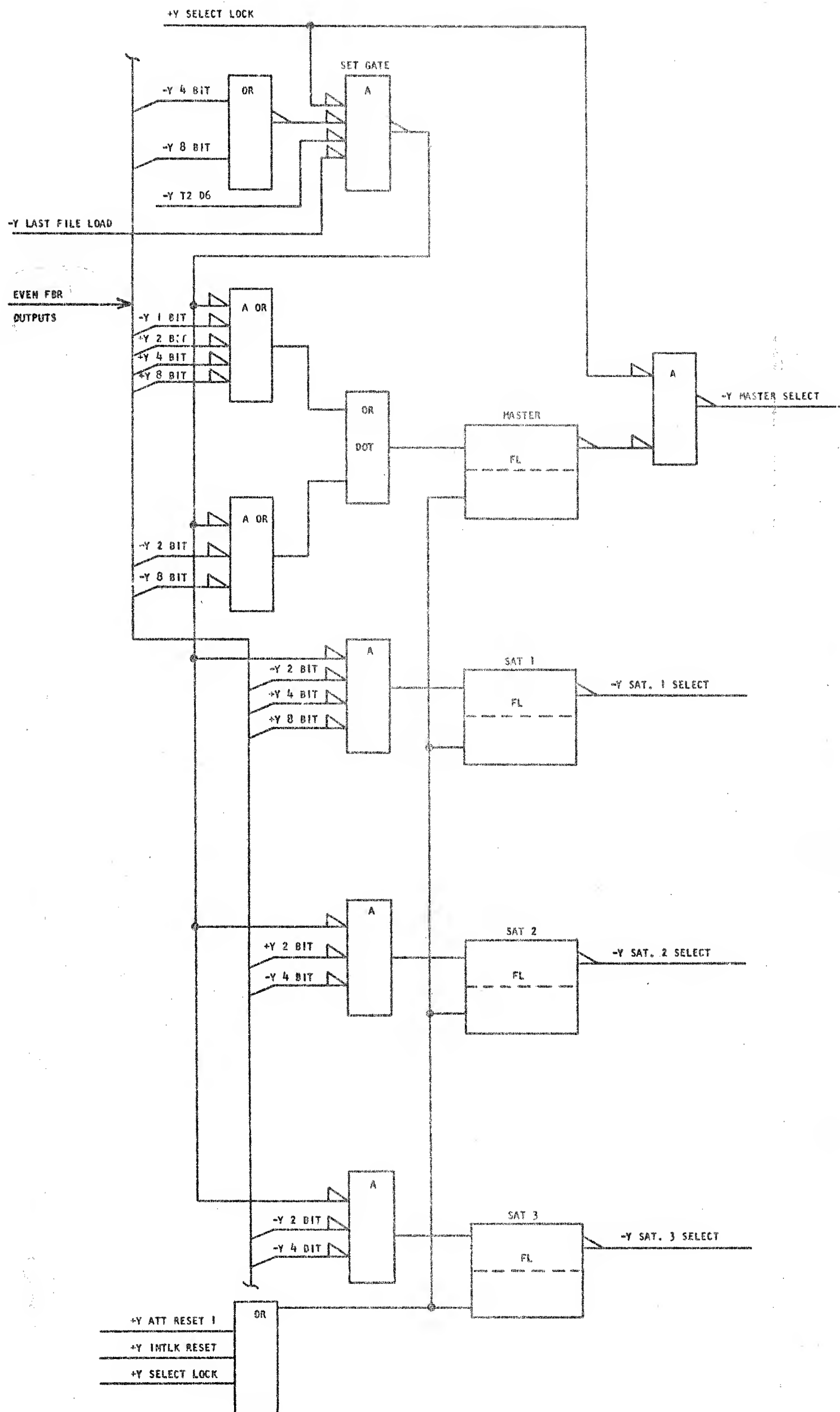


WHEN THE "SET" GATE IS SATISFIED (i.e. PLUS ON INPUT 1 AND A PLUS SHIFT ON INPUT 2) THE FLIP-FLOP IS "SET": IN THE "SET" STATE, THE OUTPUTS ASSUME THEIR INDICATE LEVELS. A NEGATIVE LEVEL AT INPUT 3 (ALL INPUTS BLOW THE CENTER LINE OF THE BLOCK ARE RESETS) RESETS THE FLIP-FLOP. IN THE RESET STATE, THE OUTPUT POLARITIES ARE OPPOSITE THOSE SHOWN.

(C)

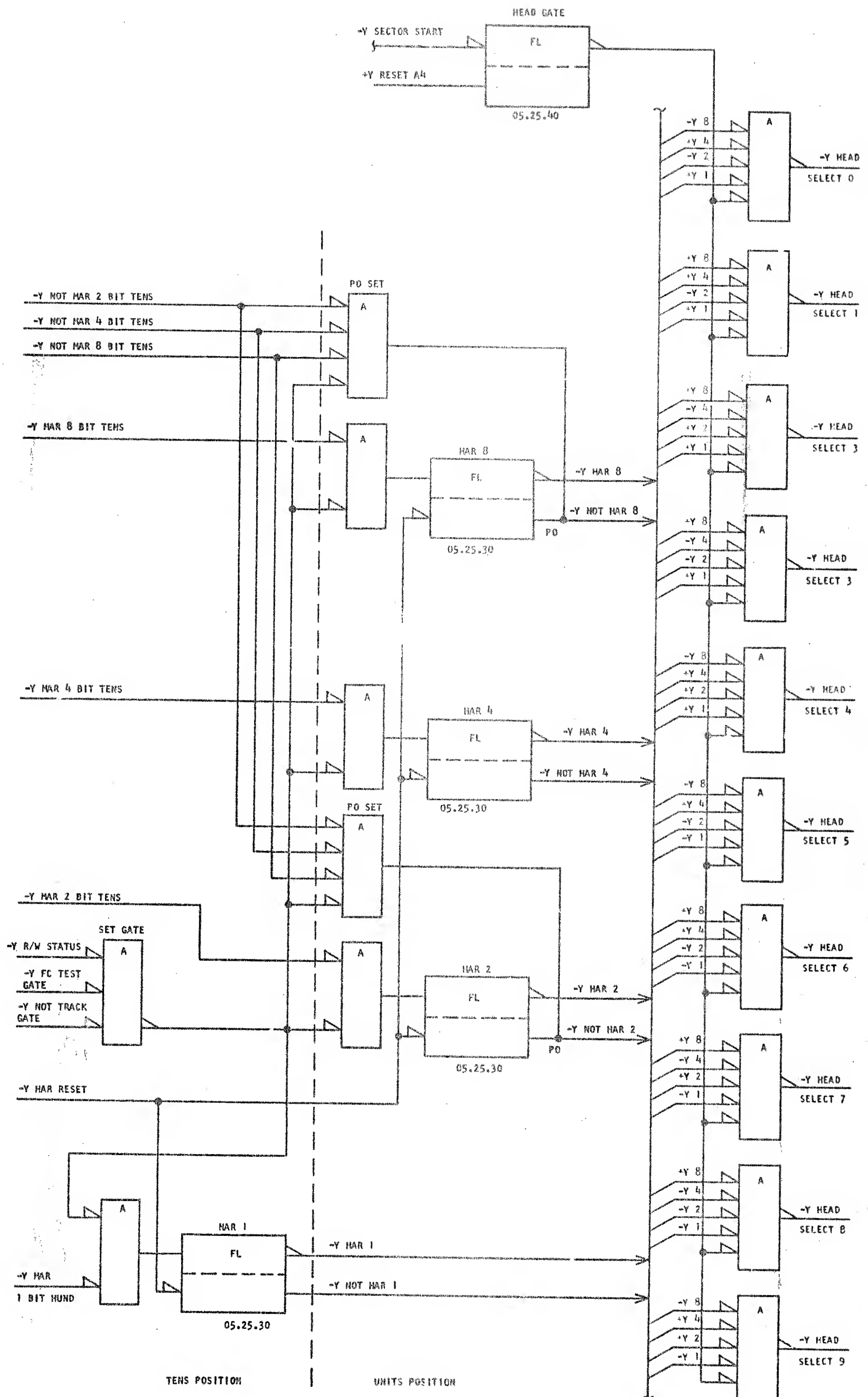


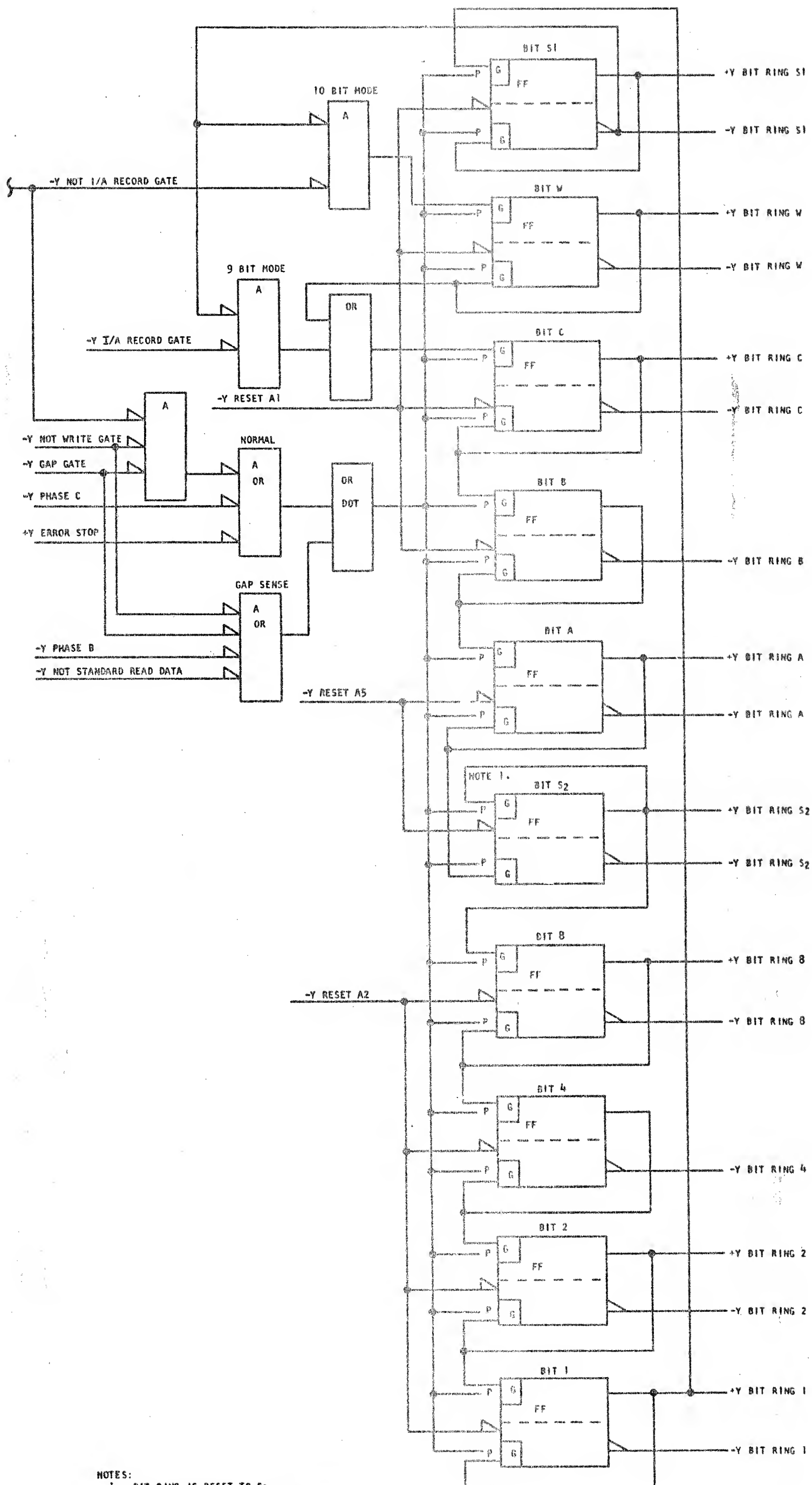
THE OUTPUT WILL ASSUME IT'S INDICATED POLARITY AFTER A TIME DELAY OF GIVEN DURATION HAS ELAPSED, SINCE THE INPUT CHANGED AS SHOWN (NEGATIVE AC SHIFT). THE OUTPUT DURATION WILL BE THE SAME AS THE INPUT DURATION UNLESS OTHERWISE NOTED.



NOTES:

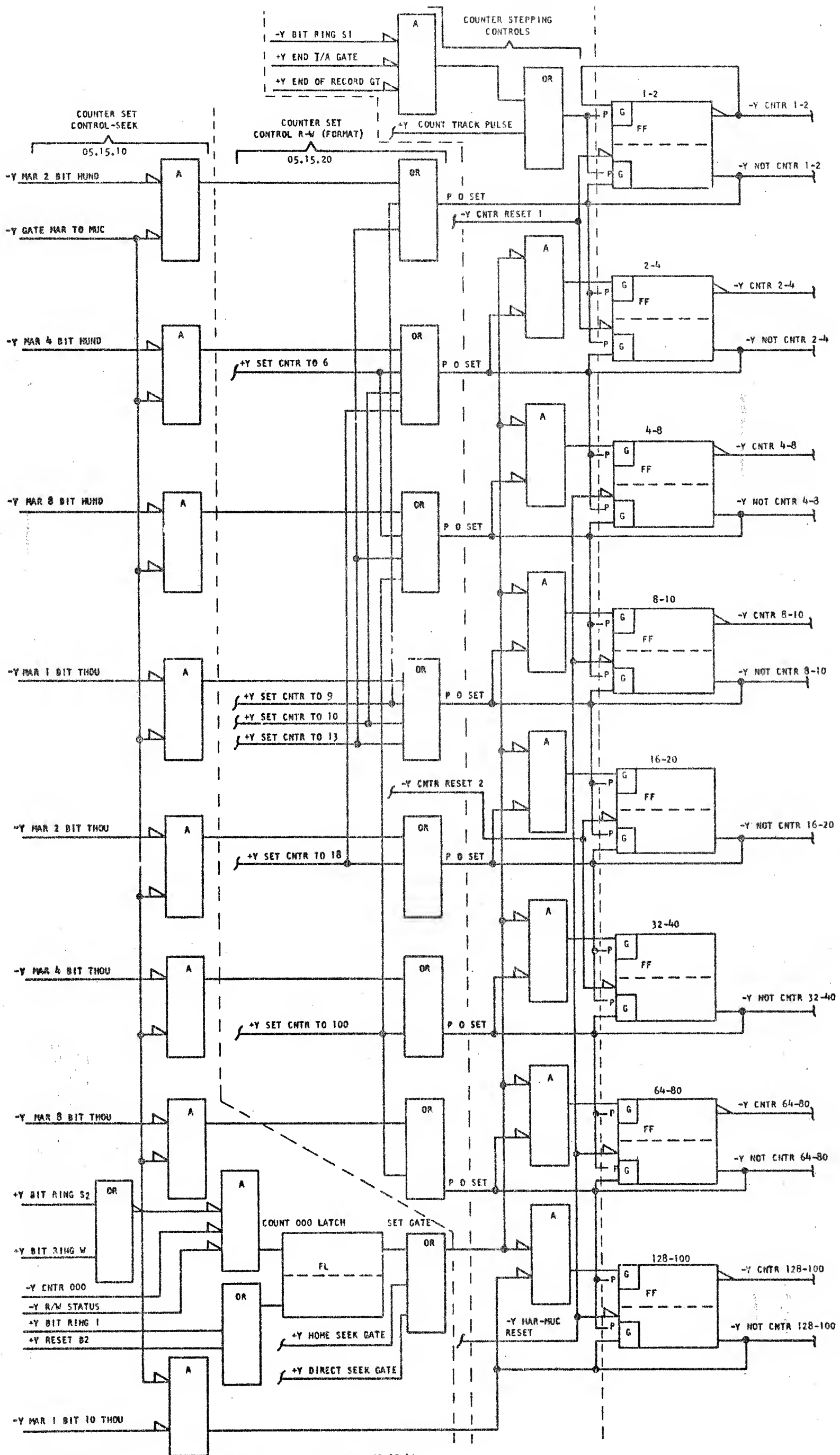
1. SEE LOGIC PAGE 05.25.20.1 FOR REFERENCE.



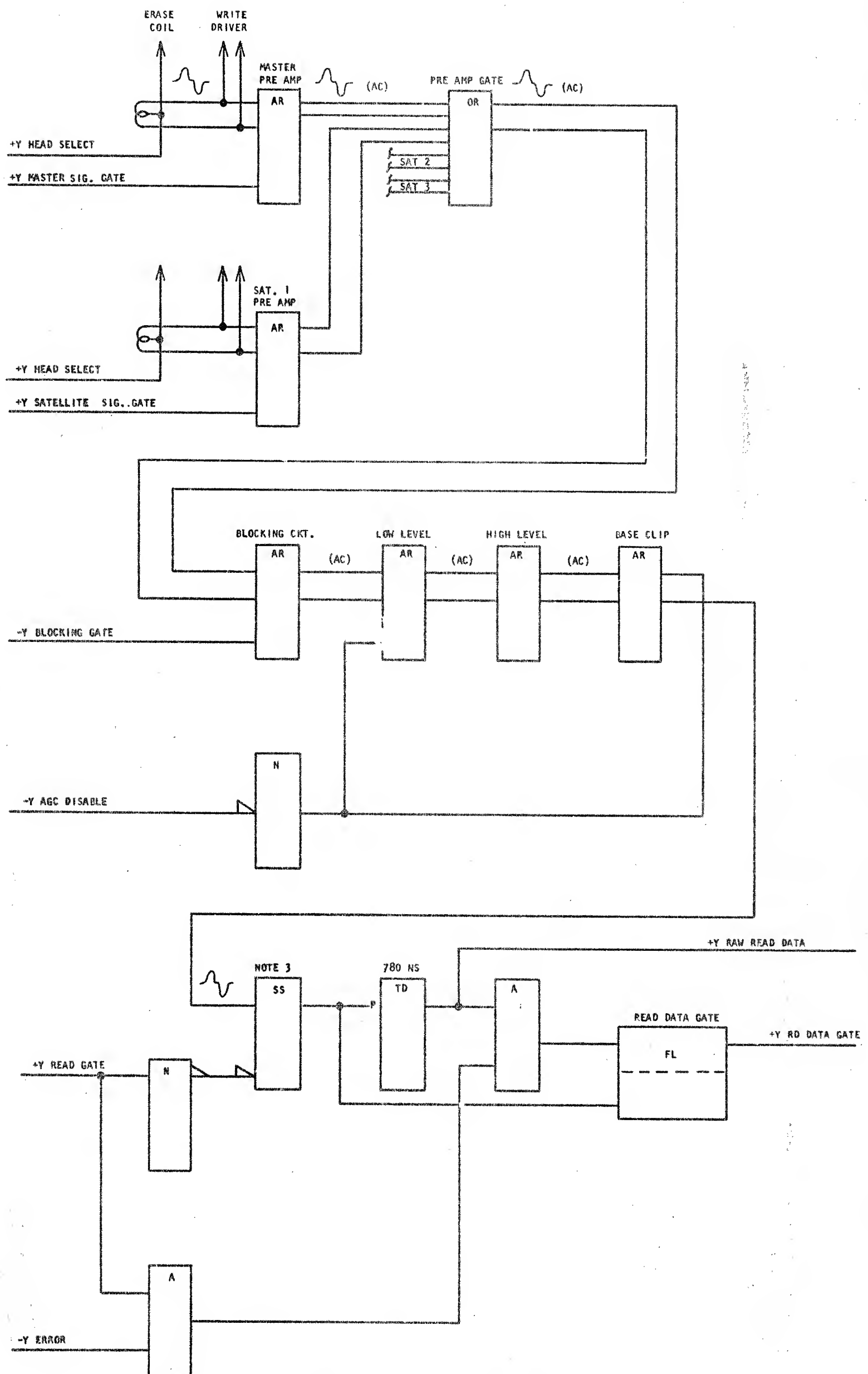


NOTES:

1. BIT RING IS RESET TO S₂.
2. SEE LOGIC PAGE 05.20.30 FOR REFERENCE.

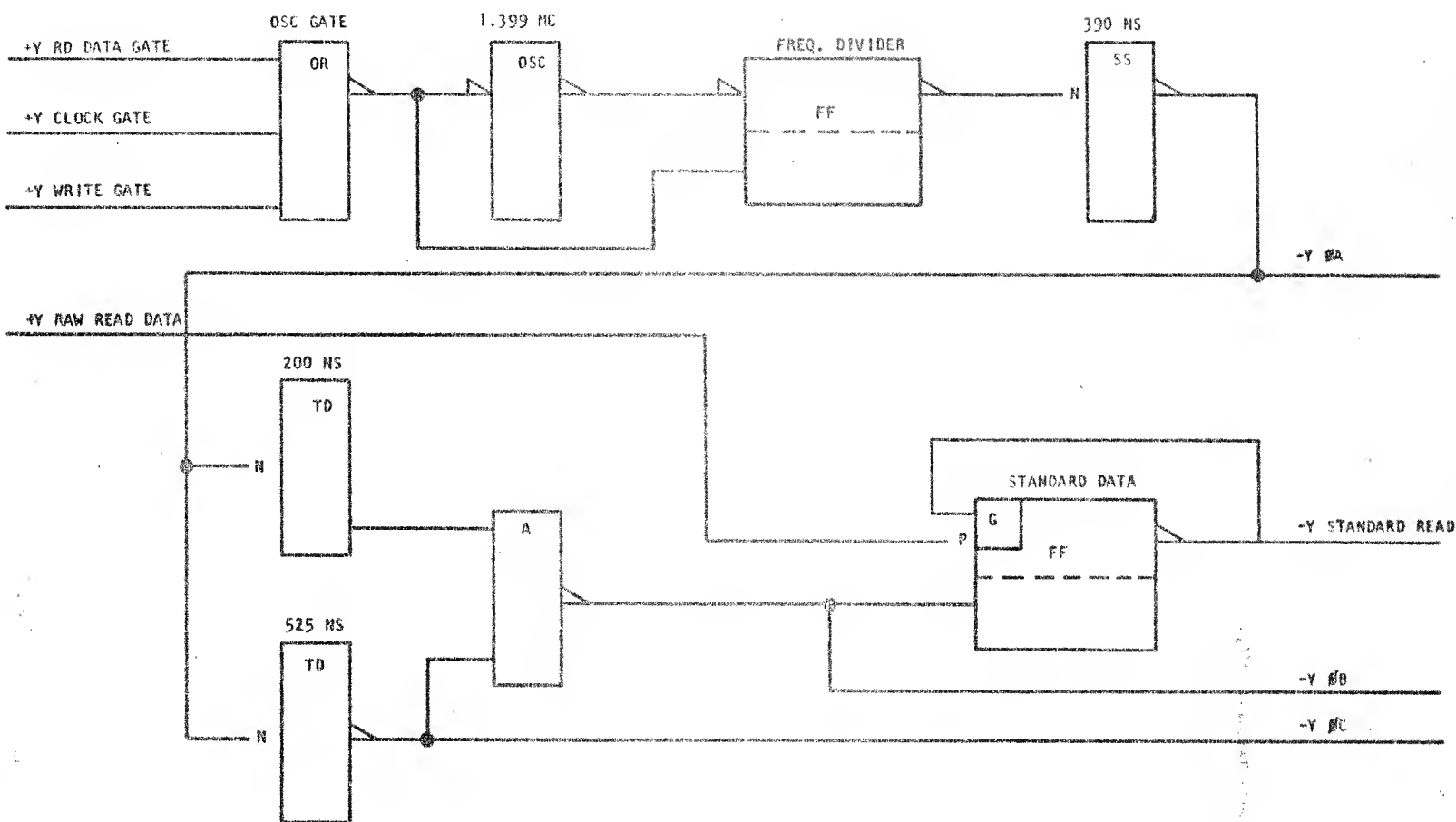


NOTE 1. REFER TO LOGIC 05.15.40

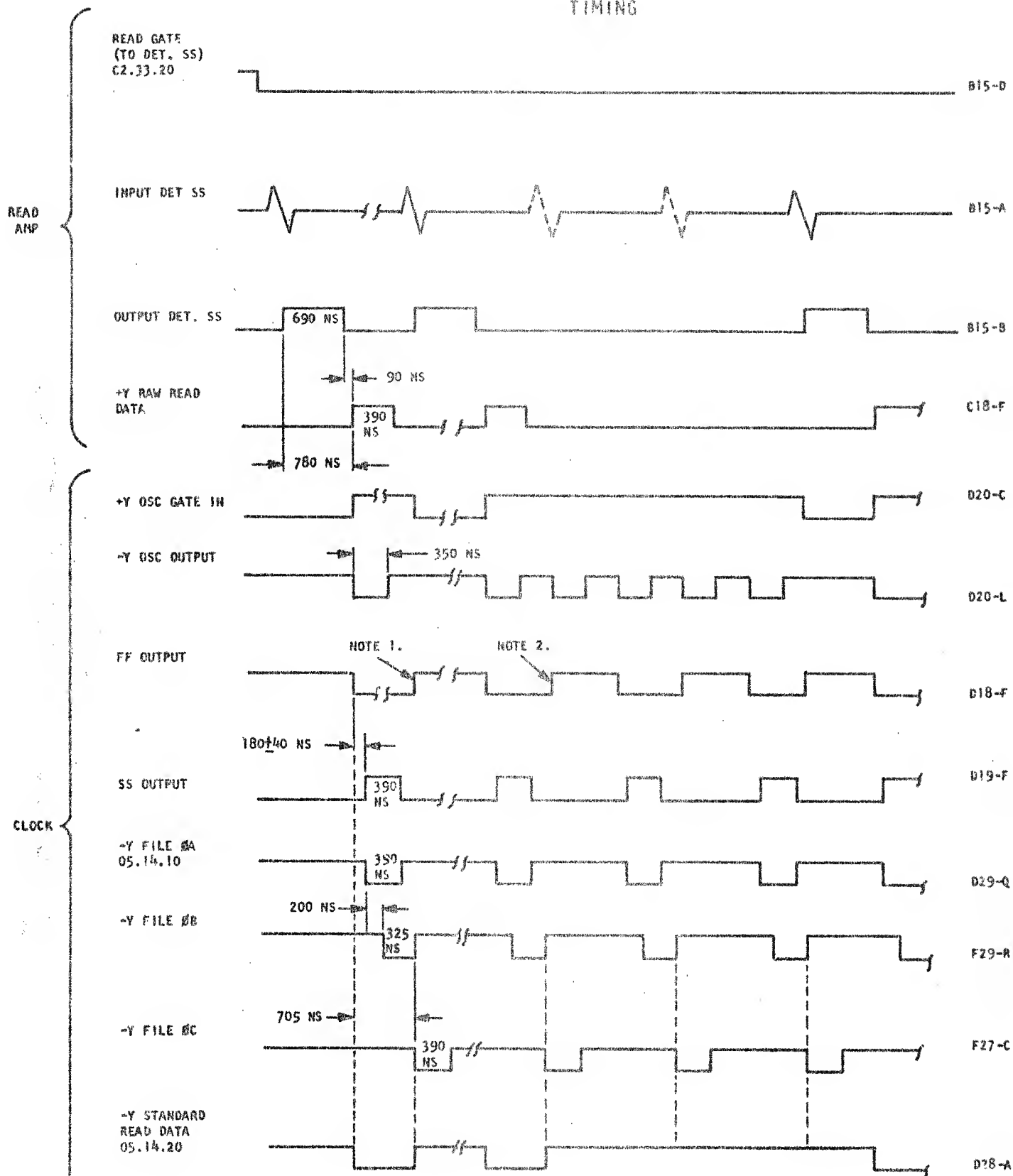


NOTES:

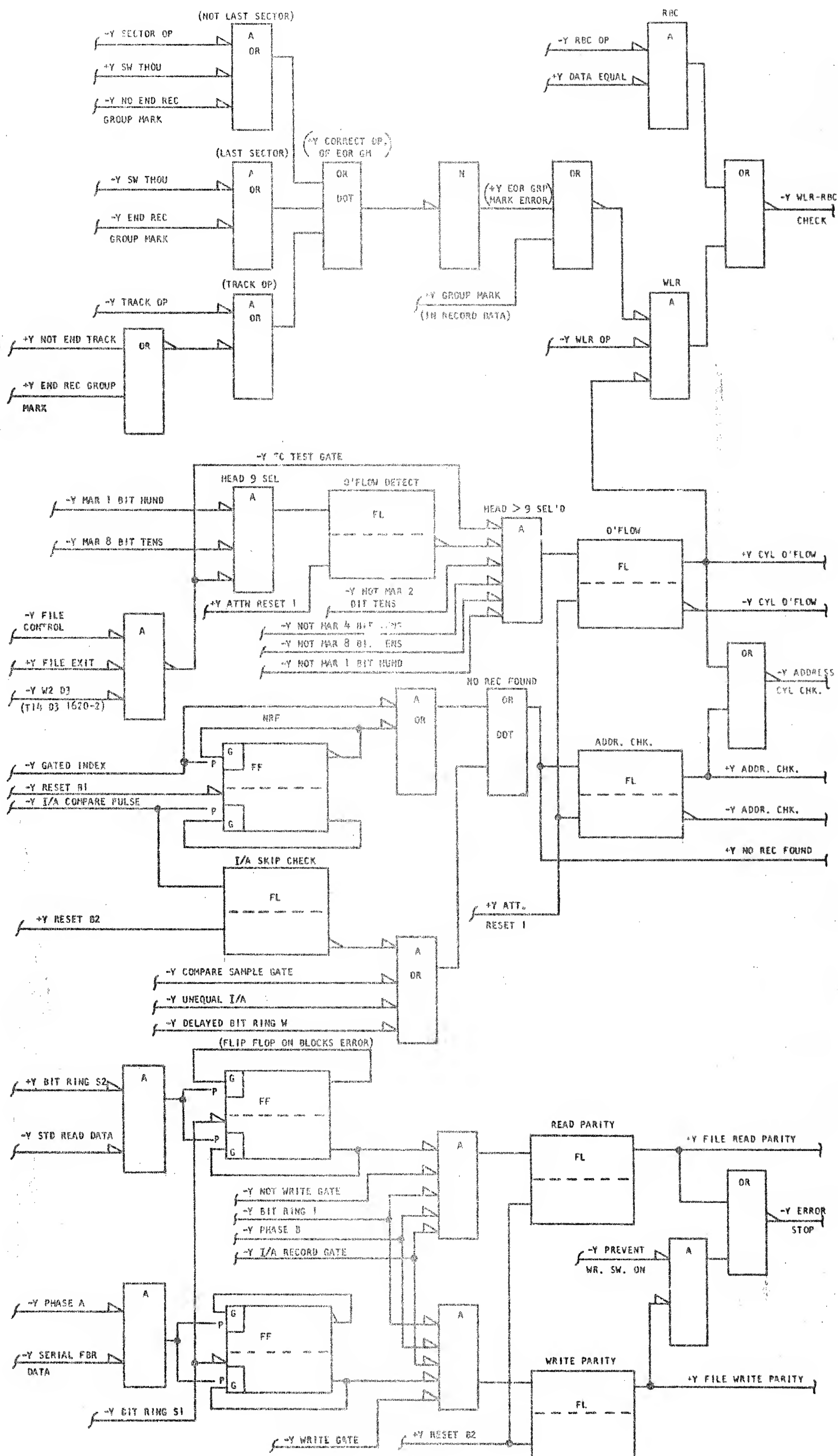
1. SEE LOGIC PAGE C2.33.20.1 FOR REFERENCE
2. SEE REFERENCE SECTION 07.XX FOR SCOPE PATTERNS OF READ & WRITE CIRCUITS
3. SEE TIMING CHART ON PAGE 06.07

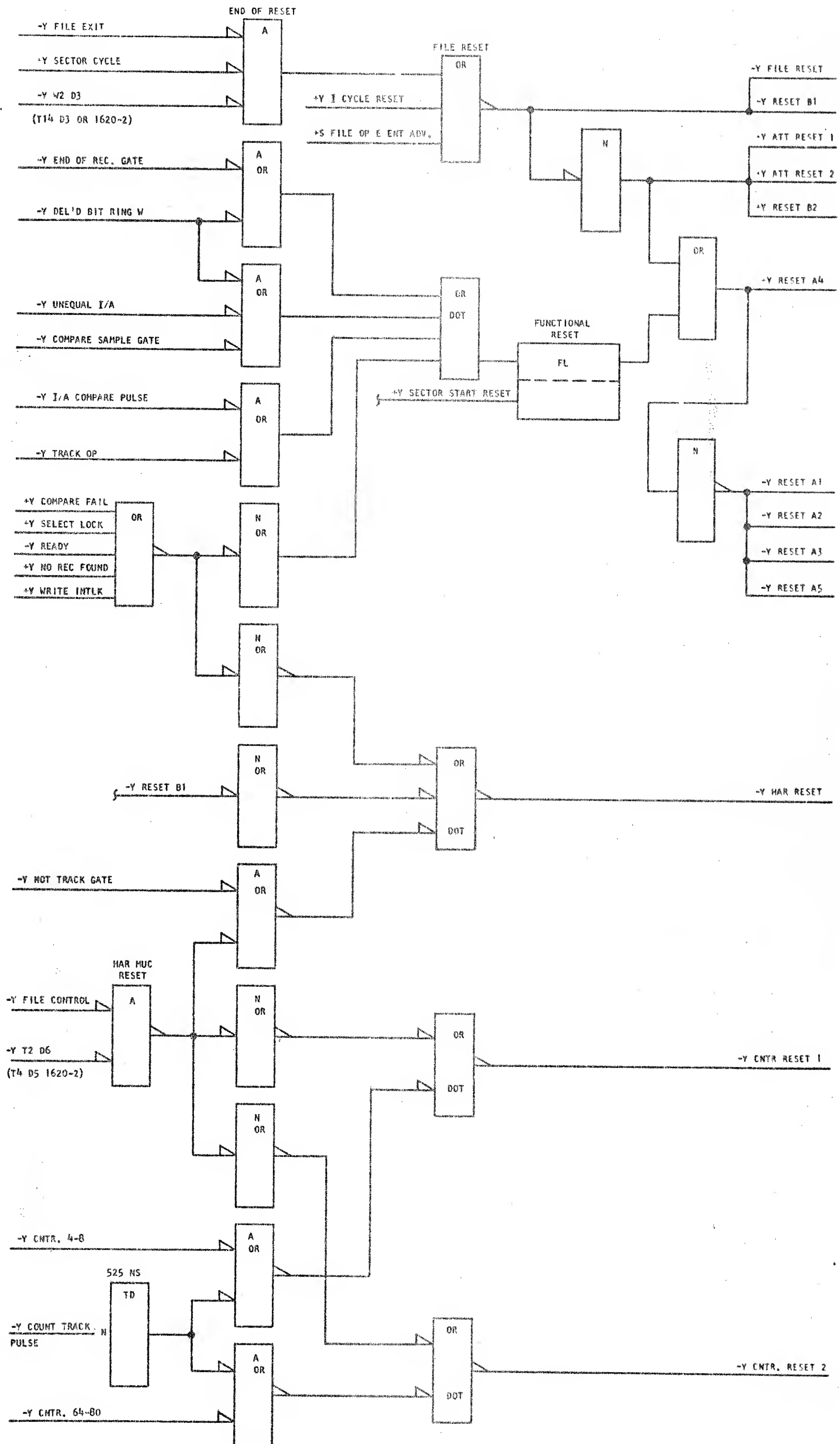


TIMING



- NOTES:
1. TURNED OFF BY OSC GATE SIG..
 2. TURNED OFF BY OSC.





REFERENCE

INDEX

CABLE CONNECTIONS, SYSTEM

1620 E & F SUFFIX	07.01
1620 G & H SUFFIX	07.02
1620 MOD II	07.03

C.E. SERVICE PANEL	07.04-07.05
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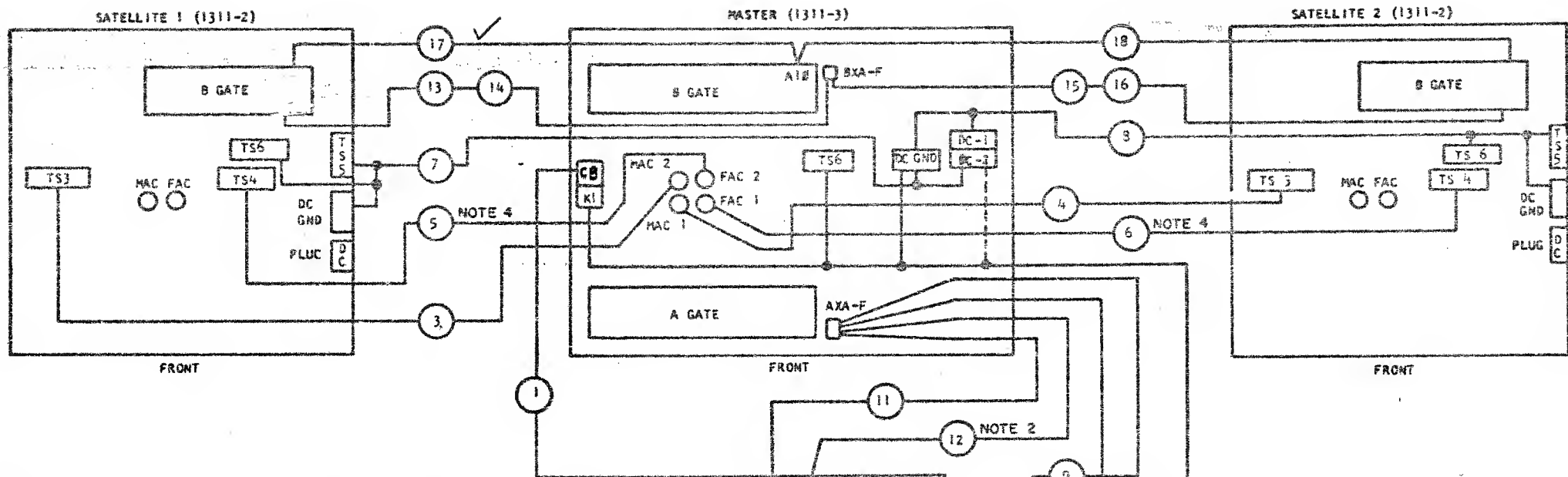
SATELLITE POWER SEQUENCE-1	07.06
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SATELLITE POWER SEQUENCE-21	07.07
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SCOPE PATTERNS

READ AMPLIFIER	07.08
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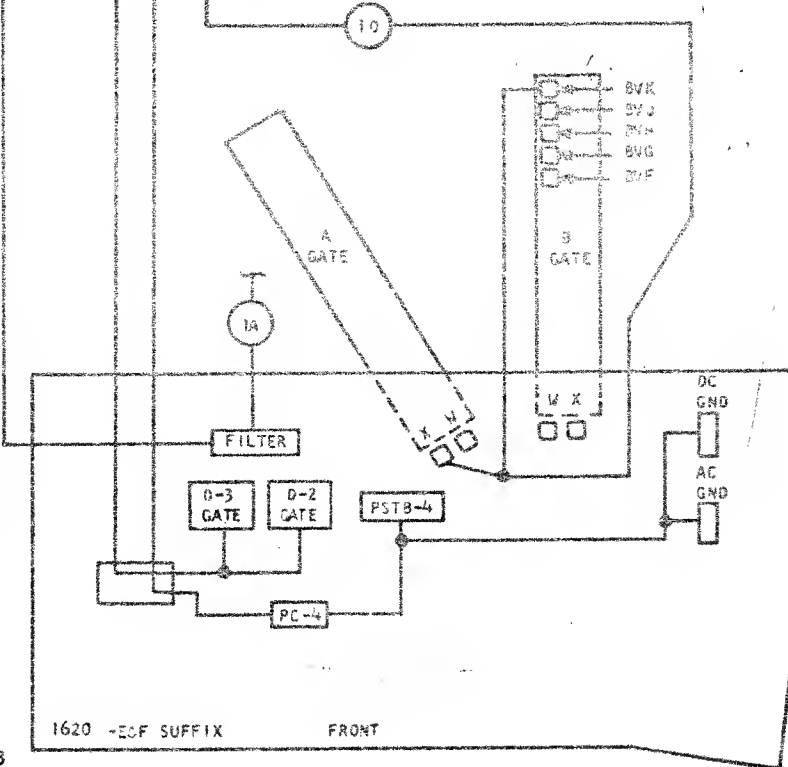
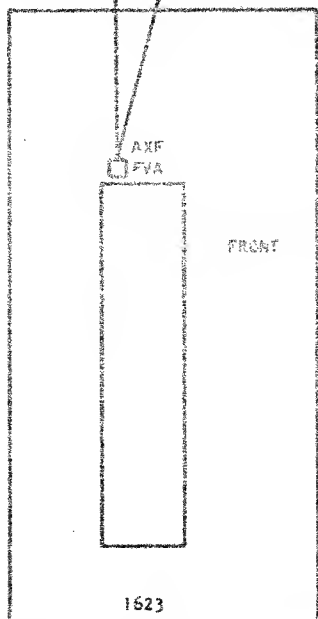
WRITE CIRCUITS	07.09
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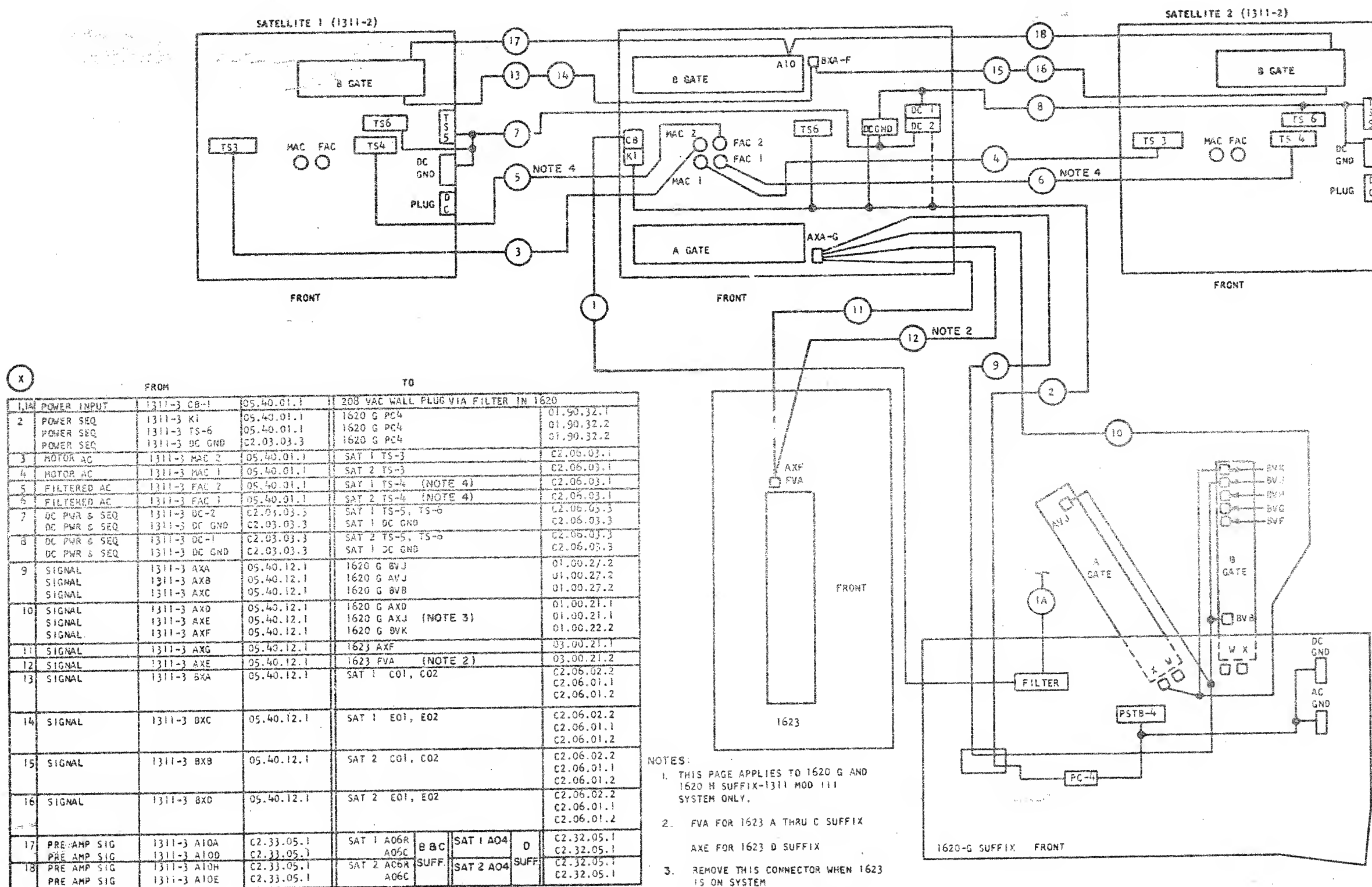


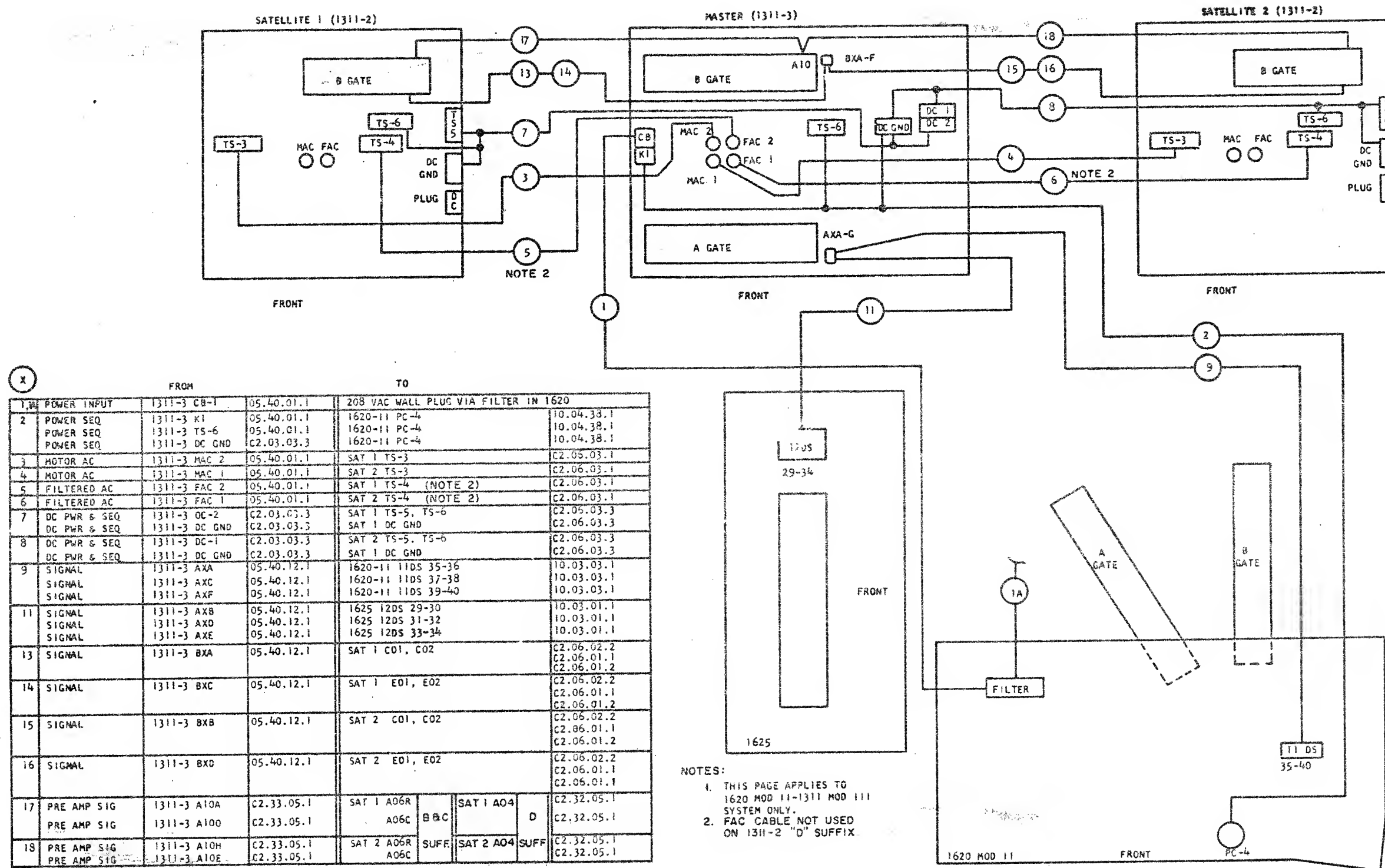
FROM	TO
1, 1A POWER INPUT	1311-3 CBI 05.40.01.1 208 VAC WALL PLUG VIA FILTER IN 1620
2 POWER SEQ	1311-3 KI 05.40.01.1 1620 PC4 01.90.32.1
3 POWER SEQ	1311-3 TS-6 05.40.01.1 1620 PC4 01.90.32.2
4 POWER SEQ	1311-3 DC GND C2.03.03.3 1620 PC4 01.90.32.2
5 MOTOR AC	1311-3 MAC2 05.40.01.1 SAT 1 TS-3 C2.06.03.1
6 MOTOR AC	1311-3 MAC1 05.40.01.1 SAT 2 TS-3 C2.06.03.1
7 FILTERED AC	1311-3 FAC2 05.40.01.1 SAT 1 TS-4 (NOTE 4) C2.06.03.1
8 FILTERED AC	1311-3 FAC1 05.40.01.1 SAT 2 TS-4 (NOTE 4) C2.06.03.1
9 DC PWR & SEQ	1311-3 DC-2 C2.03.03.3 SAT 1 TS-5, TS-6 C2.06.03.3
10 DC PWR & SEQ	1311-3 DC GND C2.03.03.3 SAT 1 DC GND C2.06.03.3
11 DC PWR & SEQ	1311-3 DC-1 C2.03.03.3 SAT 2 TS-5, TS-6 C2.06.03.3
12 DC PWR & SEQ	1311-3 DC GND C2.03.03.3 SAT 2 DC GND C2.06.03.3
13 SIGNAL	1311-3 AXA 05.40.12.1 1620 D2 A05 & B05 01.00.14.2
14 SIGNAL	1311-3 AXB 05.40.12.1 1620 D2 A04 & B04 01.00.14.2
15 SIGNAL	1311-3 AXC 05.40.12.1 1620 D3 A05 & B05 01.00.14.3
16 SIGNAL	1311-3 AXD 05.40.12.1 1620 AXD 01.00.21.1
17 SIGNAL	1311-3 AXE 05.40.12.1 1620 AXJ (NOTE 3) 01.00.21.1
18 SIGNAL	1311-3 AXF 05.40.12.1 1620 BVK 01.00.22.2
19 SIGNAL	1311-3 AXG 05.40.12.1 1623 AXF 03.00.21.1
20 SIGNAL	1311-3 AXH 05.40.12.1 1623 FVA (NOTE 2) 03.00.21.2
21 SIGNAL	1311-3 BXA 05.40.12.1 SAT 1 C01, C02 C2.06.02.2
22 SIGNAL	1311-3 BXC 05.40.12.1 SAT 1 E01, E02 C2.06.01.1
23 SIGNAL	1311-3 BXD 05.40.12.1 SAT 1 E01, E02 C2.06.01.2
24 SIGNAL	1311-3 BXB 05.40.12.1 SAT 2 C01, C02 C2.06.02.2
25 SIGNAL	1311-3 BXD 05.40.12.1 SAT 2 E01, E02 C2.06.01.1
26 SIGNAL	1311-3 BXD 05.40.12.1 SAT 2 E01, E02 C2.06.01.2
27 PRE AMP SIG	1311-3 A10A C2.33.05.1 SAT 1 A05R B&C SAT 1 A04 D C2.32.05.1
28 PRE AMP SIG	1311-3 A10D C2.33.05.1 SAT 1 A05C B&C SAT 1 A04 D C2.32.05.1
29 PRE AMP SIG	1311-3 A10H C2.33.05.1 SAT 2 A05R SUFF SAT 2 A04 SUFF C2.32.05.1
30 PRE AMP SIG	1311-3 A10E C2.33.05.1 SAT 2 A05C SUFF SAT 2 A04 SUFF C2.32.05.1

NOTES:

1. THIS PAGE APPLIES TO 1620 E & F SUFFIX-1311 III SYSTEMS ONLY
2. FVA FOR 1623 A THRU C SUFFIX AXE FOR 1623 D SUFFIX
3. REMOVE THIS CONNECTOR WHEN 1623 IS ON SYSTEM
4. FAC CABLE NOT USED ON 1311-2 "D" SUFFIX.







THE FOLLOWING IS A DESCRIPTION OF THE FUNCTIONS PROVIDED BY THE C. E. TEST PANEL LOCATED ON "B" GATE. THE DESCRIPTIONS ARE LISTED FROM THE TOP OF THE PANEL:

1. INDEX HUB:

THIS HUB PROVIDES A GATED INDEX TO BE USED FOR SYNCING. THE MODULE MUST BE SELECTED TO OBTAIN THIS IMPULSE AND ON MULTI-FILE SYSTEMS THE ACTUAL DISK DRIVE BEING USED WILL PROVIDE THE INDEX.

2. SYNC GATE HUB:

THIS HUB IS THE OUTPUT OF THE CE "AND" CIRCUIT (SHOWN ON 05.04.10.1). THE INPUTS TO THE CE "AND" ARE THE TWO FORMAT SWITCHES LISTED BELOW AND THE ADDITIONAL INPUTS THAT CAN BE EXTERNALLY JUMPED BY C.E. ON "B" SUFFIX FILES THIS CIRCUIT IS A 10 WAY "AND". ON "C" SUFFIX FILES THIS CIRCUIT IS A 5 WAY "AND".

3. FORMAT SWITCHES:

THE UPPER FORMAT SWITCH IS A ROTARY SWITCH THAT CAN SELECT ANY ONE OF THE FORMAT GATES INTO ONE INPUT OF THE C.E. "AND" CIRCUIT. THE LOWER FORMAT SWITCH CAN SELECT EITHER THE ADDRESS OR NOT ADDRESS GATES FOR THE SECOND INPUT TO THE C.E. "AND" (05.04.10.1).

4. ANY TEST SWITCH ON LIGHT (C SUFFIX ONLY).

THIS LIGHT INDICATES THAT ONE OF THE C.E. TEST SWITCHES IS ON. THE LIGHT MUST BE OFF WHEN SERVICING IS COMPLETED.

5. INDEX LOCK SWITCH (ON B SUFFIX FILES ONLY)

THE INDEX LOCK SWITCH PROVIDES A METHOD FOR USING THE INDEX SYNC HUB ON A SECTOR MODE INSTRUCTION SO THAT THE FIRST SECTOR CAN BE OBSERVED. WHEN THE INDEX LOCK SWITCH IS TURNED ON, THE FCU WILL RECOGNIZE ONLY THE INDEX PULSE RATHER THAN THE OTHER SECTOR PULSES. TO USE THE INDEX LOCK SWITCH, PROGRAM THE USING SYSTEM TO DO A SECTOR OPERATION USING ANY FIRST SECTOR ADDRESS AS A STARTING ADDRESS. FOLLOW THE FILE INSTRUCTION WITH A BRANCH TO REPEAT THE FILE INSTRUCTION. THE SECTOR COUNT IN THE FILE INSTRUCTION NEED ONLY BE 001, AS ONLY THE FIRST SECTOR WILL BE SEEN.

THE FIRST SECTOR MAY NOW BE OBSERVED BY TURNING ON THE INDEX LOCK SWITCH AND SYNCING THE SCOPE ON THE INDEX SYNC HUB OUTPUT. THE GATED INDEX PULSE AVAILABLE AT THE INDEX SYNC HUB IS NOW A SOLID SYNC PULSE THAT CAN BE USED TO ALLOW ANALYSIS OF FORMAT AND CONTROL GATES ON A SECTOR OPERATION.

THE INDEX LOCK SWITCH ACCOMPLISHES THE FUNCTIONS DESCRIBED ABOVE BY CLAMPING ON THE INDEX LOCK LATCH. THE LATCH OUTPUT INHIBITS THE NORMAL SECTOR OPERATION SECTOR START PULSE AND ALLOWS ONLY THE GATED INDEX PULSE TO GENERATE A SECTOR START PULSE. IN ADDITION, THE NRE CIRCUIT IS DISABLED FORCING THE PROGRAMMED FILE OP INTO A CONTINUOUS LOOP REGARDLESS OF WHETHER AN IA COMPARE PULSE IS DEVELOPED OR NOT. THE INDEX LOCK INDICATOR REMAINS ON AS LONG AS THE SWITCH IS ON.

INDEX LOCK FUNCTION (C SUFFIX & LATER)

ON "C" SUFFIX FILES THE INDEX LOCK FUNCTION IS INCORPORATED INTO THE COMPARE DISABLE SWITCH. WHEN THE COMPARE DISABLE SWITCH IS PULLED OUT AND A TRACK OPERATION IS BEING PERFORMED, THE COMPARING OF ADDRESSES IS ELIMINATED (THE SAME AS ON PREVIOUS SUFFIXES). WITH THE COMPARE DISABLE SWITCH PULLED OUT WHEN PERFORMING A SECTOR OPERATION THE FILE WAITS UNTIL INDEX TO PERFORM THE FIRST ADDRESS COMPARE. THIS IS ACCOMPLISHED BY THE C. E. INDEX START LATCH ON 05.21.10.1. THE NORMAL SECTOR DELAY WILL BE ACCOMPLISHED BEFORE THE ADDRESS COMPARING STARTS AT INDEX. ALL OTHER OPERATIONS ARE NORMAL AND ANY NUMBER OF SECTORS CAN BE READ OR WRITTEN.

THIS SERVICE AID WILL HELP WHEN SCOPING A PROBLEM THAT HANGS-UP THE FORMAT, OR AN ERROR AN ADDRESS COMPARING.

THE COMPARE DISABLE SWITCH IS RESET WHEN THE "B" GATE IS CLOSED.

(CONTINUED)

6. PREVENT WRITE SWITCH (C SUFFIX ONLY)

WHEN TURNED ON, THIS SWITCH WILL PERMIT THE FILE TO PERFORM ALL NORMAL WRITE FUNCTIONS EXCEPT ACTUALLY DRAWING WRITE AND ERASE CURRENT THROUGH THE HEAD. THIS WILL PERMIT SCOPING OF TROUBLES THAT MODIFY THE ADDRESSES ON THE DISK PREVENTING ANY FURTHER EQUAL ADDRESS COMPARES.

7. CLOCK GATE SWITCH.

THE CLOCK GATE SWITCH ALLOWS COMPLETE CLOCK SCOPING BY CAUSING R/W OSCILLATOR, THE BIT RING AND MUC COUNTER TO RUN. TURNING ON THE CLOCK GATE SWITCH FORCES ON CLOCK GATE WHICH ALLOWS THE OSCILLATOR TO FREE RUN. THE OSCILLATOR OUTPUT STEPS THE BIT RING AND THE BIT RING OUTPUT STEPS MUC. THE CLOCK GATE SWITCH ALSO CLAMPS OFF THE "A" RESETS ALLOWING BIT RING SEQUENCING. THE SWITCH ALSO FORCES A WRITE INTERLOCK BY WAY OF THE ILLEGAL OP LINE. THIS PREVENTS THE DEVELOPMENT OF WRITE STATUS IN THE FILE AND ALSO FORCES A CLOCK STOP SIGNAL TO THE 1620, THUS PROTECTING DATA IN MEMORY AND ON THE FILE. THE CLOCK GATE INDICATOR REMAINS ON AS LONG AS THE SWITCH IS ON.

8. INDICATOR LAMPS

THE INDIVIDUAL LAMPS ARE ON WHENEVER THE NAMED GATE IS UP (05.04.05.1). A SMALL CURRENT IS CONTINUOUSLY DRAWN THROUGH THE BULBS TO INCREASE BULB LIFE. THIS CAUSES THE BULB FILAMENTS TO GLOW SLIGHTLY.

9. ERROR STOP SWITCH (C SUFFIX ONLY)

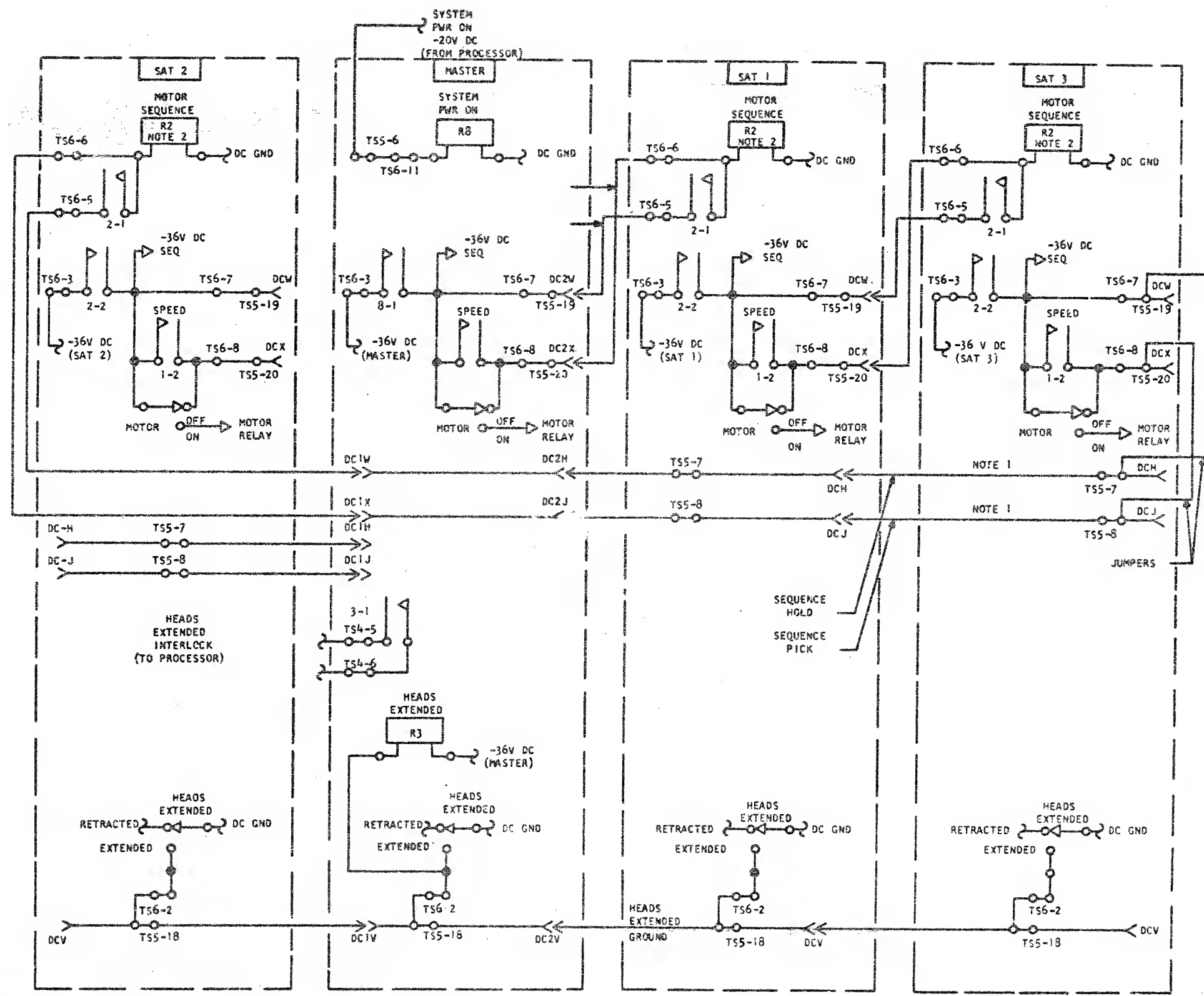
THIS SWITCH WAS ADDED TO ALLOW THE CUSTOMER ENGINEER TO STOP THE BIT RING ON THE FILE WHEN A PARITY ERROR IS DETECTED.

WHEN TURNED ON, THIS SWITCH WILL STOP THE FILE AT PHASE B OF BIT RING 1 OF THE CHARACTER WITH INCORRECT PARITY. THIS WILL PREVENT ANY FURTHER STROBES TO THE 1620. THE 1620 WILL STOP AT THE ADDRESS OF THE INCORRECT CHARACTER. THIS WILL PERMIT THE C.E. TO SCOPE THE FILE BUFFER REGISTERS, CONTROL LINES AND COUNTERS WITH THE ERROR CONDITIONS PRESENT.

THIS ERROR STOP CONDITION MUST BE RELEASED FROM THE CPU CONSOLE BY DEPRESSING THE RELEASE OR RESET KEY. IF THE ERROR STOP SWITCH IN THE FILE IS TURNED OFF WHEN "ERROR STOPPED" THE BIT RING AND FILE DATA WILL NOT BE IN STEP, AND A RANDOM COMBINATION OF INCORRECT DIGITS WILL RESULT.

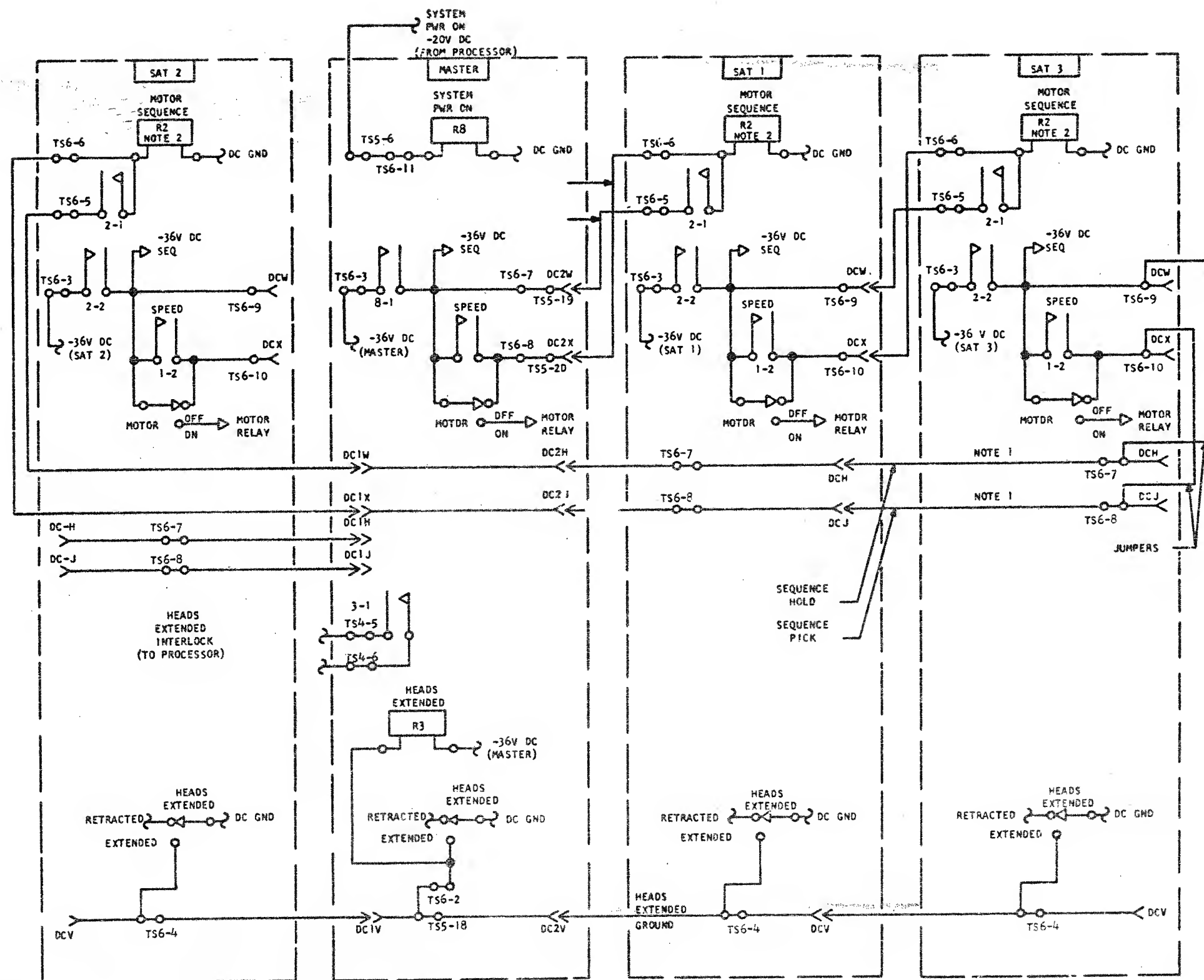
THE FILE WILL STOP ON READ PARITY, BUT THE PREVENT WRITE SWITCH MUST BE TURNED ON IN ORDER FOR THE ERROR STOP SWITCH TO FUNCTION ON A WRITE OPERATION. THIS IS NECESSARY TO PREVENT THE ERASING OF THE ENTIRE TRACK WHEN THE BIT RING IS STOPPED.

AN ADDITIONAL STOP PIN HAS BEEN PROVIDED THAT WILL ENABLE THE C.E. TO ERROR STOP THE FILE ON A SELECTED CONDITION (05.30.30.1).

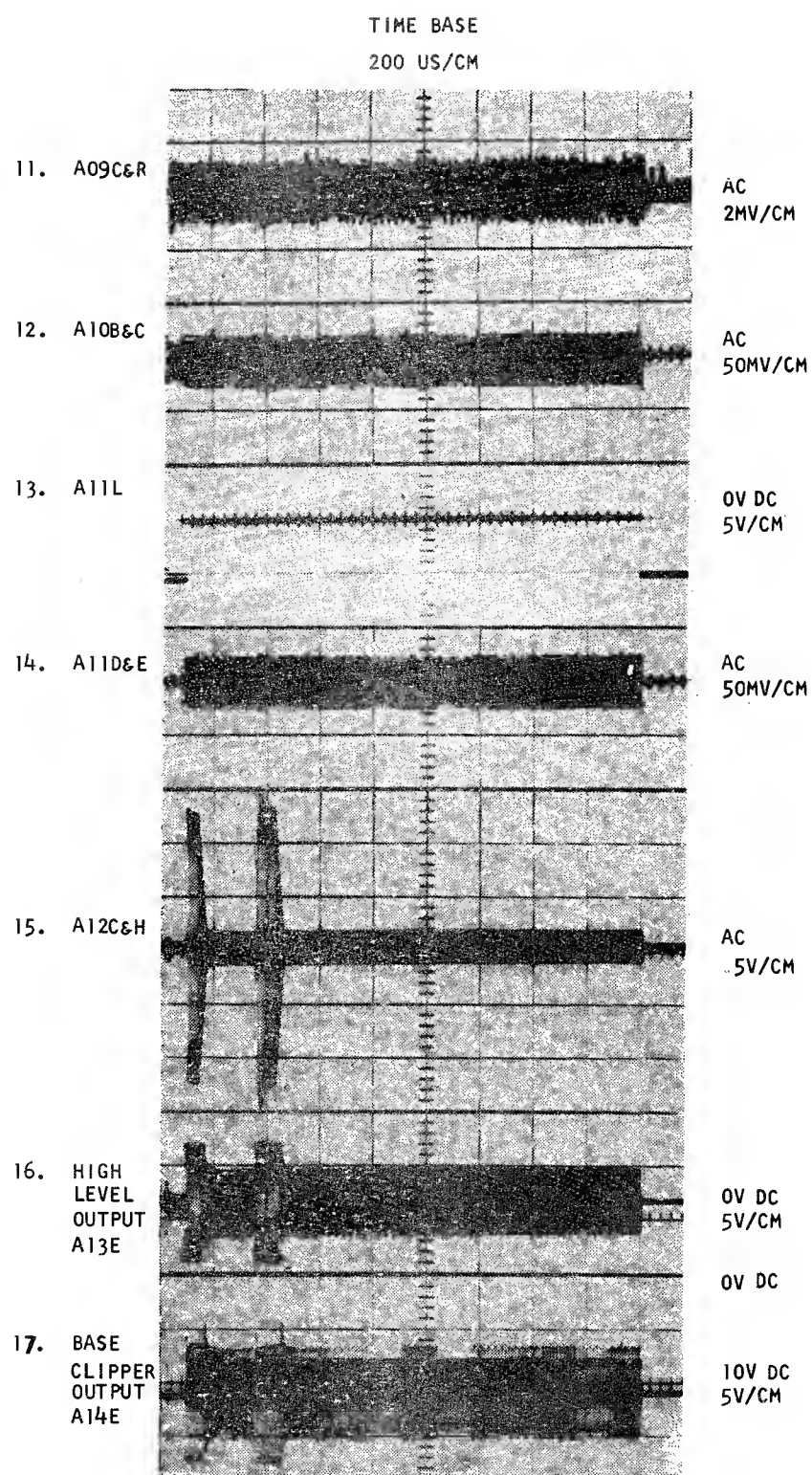
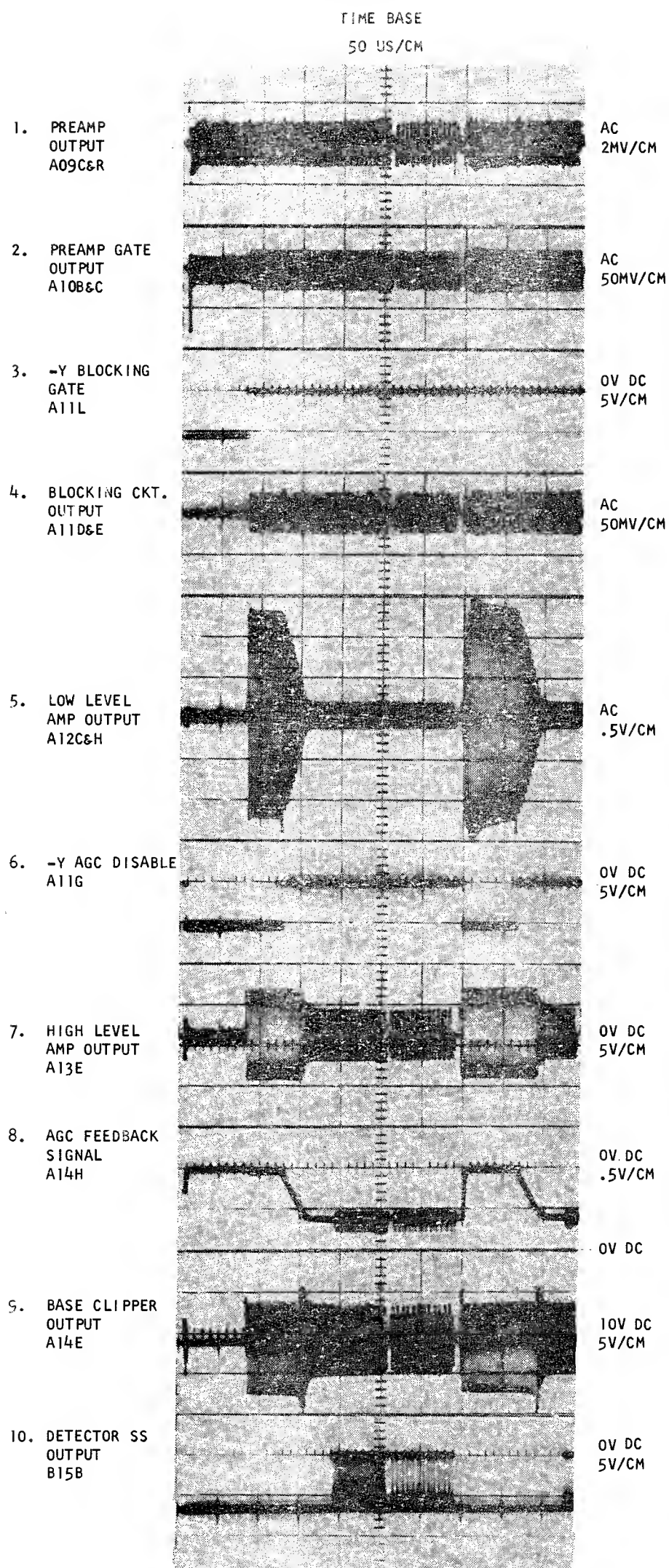


NOTE 1: MOTOR SEQUENCE LOOP
NOTE 2: POWERED BY ISOLATED -36V DC FROM PREVIOUS FILE

WIRING FOR 3
SATELLITES

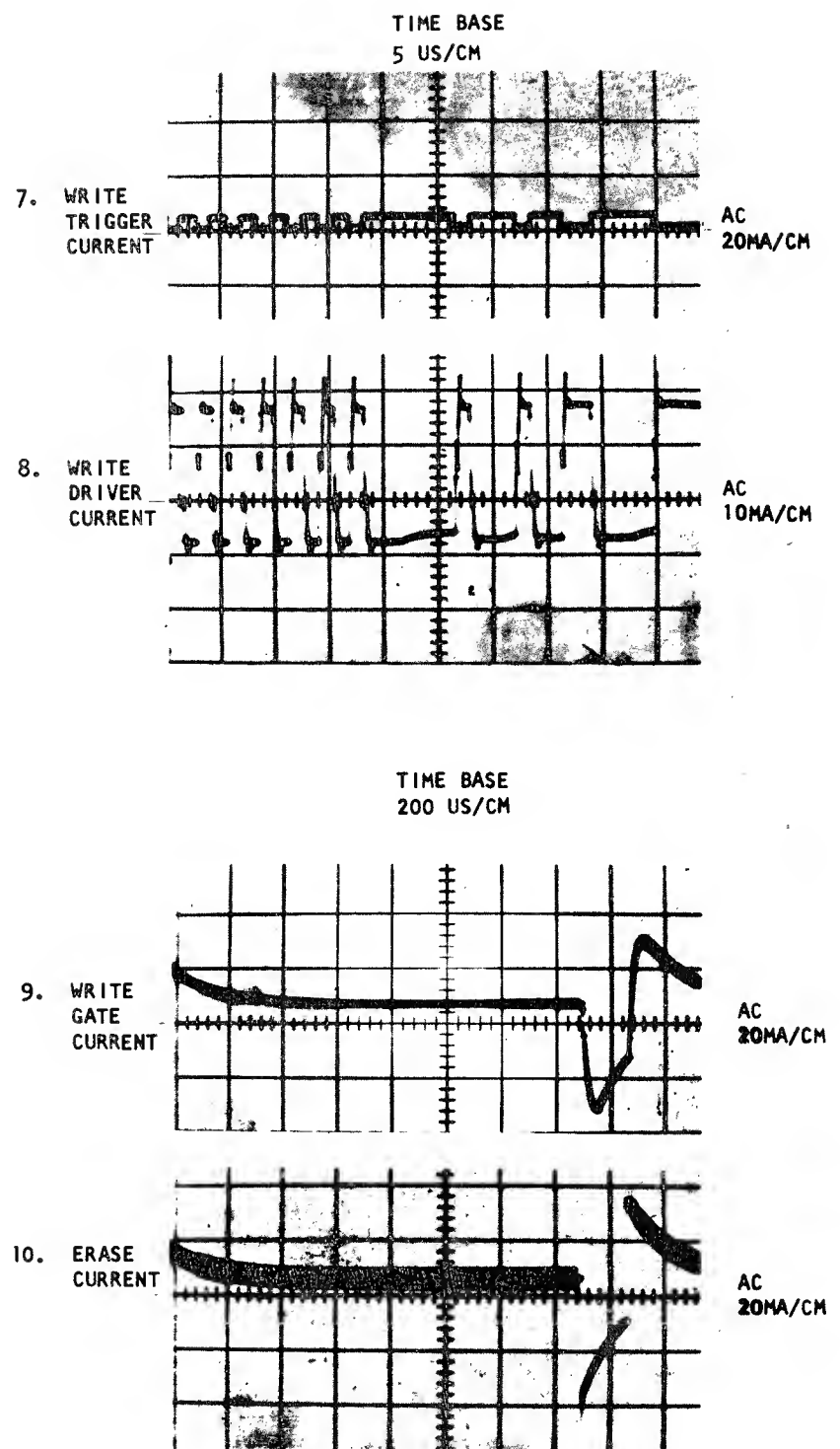
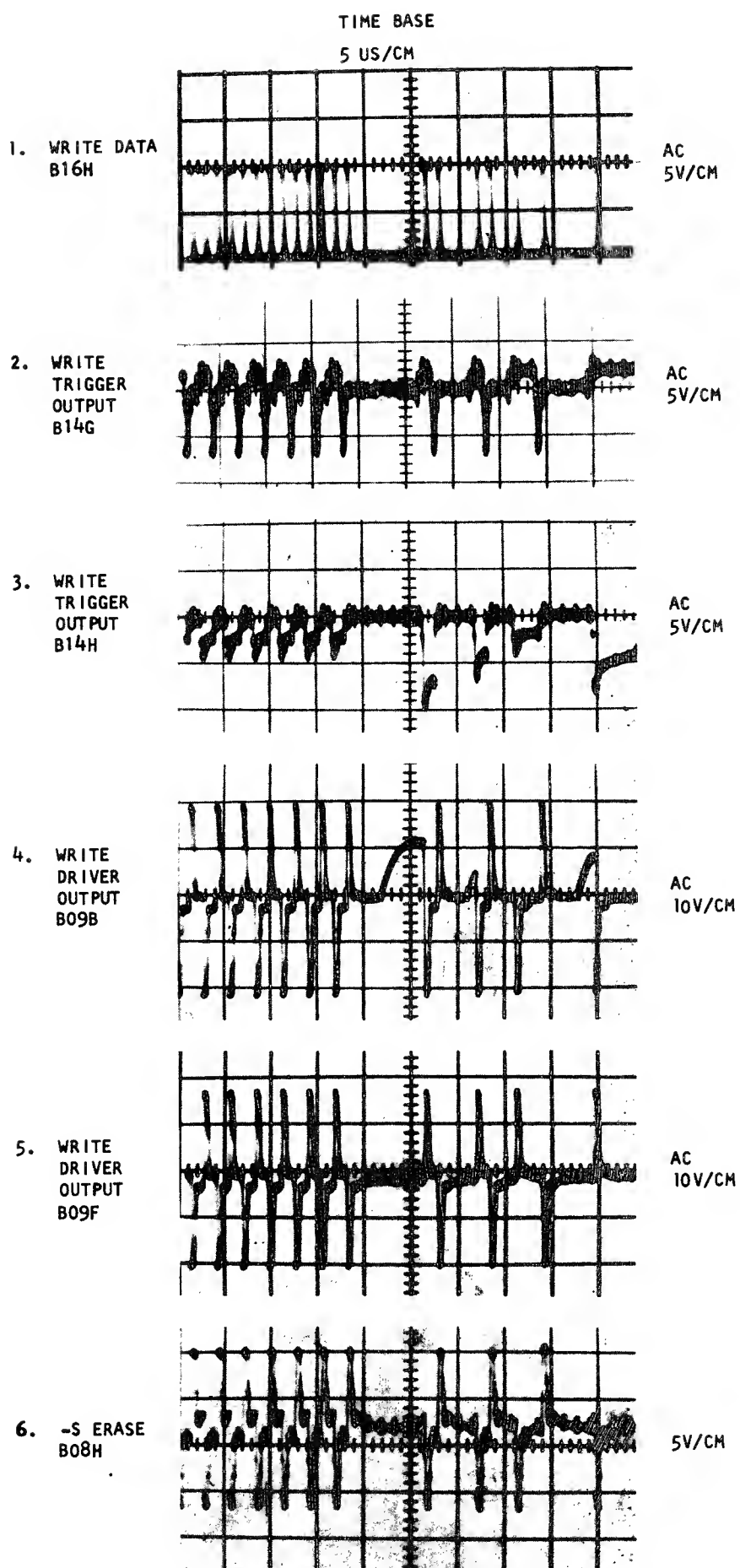


NOTE 1: MOTOR SEQUENCE LOOP
NOTE 2: POWERED BY ISOLATED -36V DC FROM PREVIOUS FILE



NOTES:

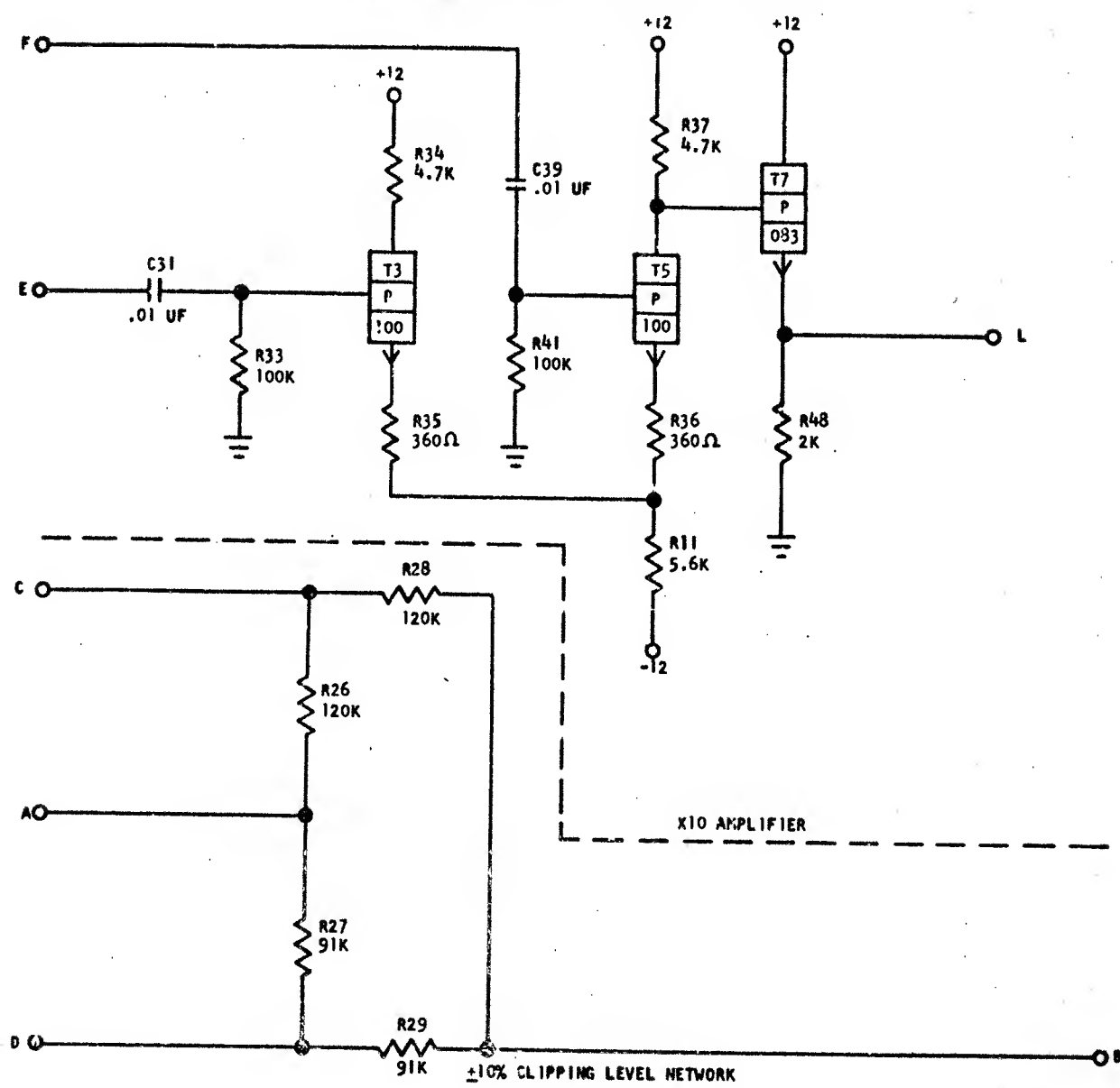
1. SCOPE: TEKTRONIX 535
 - (a) PREAMP 53/54 D USED FOR TRACES 1. AND 11. ONLY. INPUTS, AC A-B.
 - (b) PREAMP CA USED FOR ALL OTHER TRACES: AC ADDED, CHANNEL 2 INV, USED ON 2, 4, 5, 12, 14 & 15. A SINGLE PROBE WAS USED ON 7, 9, 16 & 17.
2. SYNC: EXTERNAL MINUS AT D11F ("INDEX" ON SPEED DETECT CARD).
3. PROBES: DIRECT (X1); SHIELD GROUNDED AT PROBE TIP ON ANY R/W GROUND.
4. DISPLAY: TRACES 1. THROUGH 10., ADDRESS AGC, I/A & RECORD AGC: TRACES 11. THROUGH 17., ONE SECTOR OF OPERATION



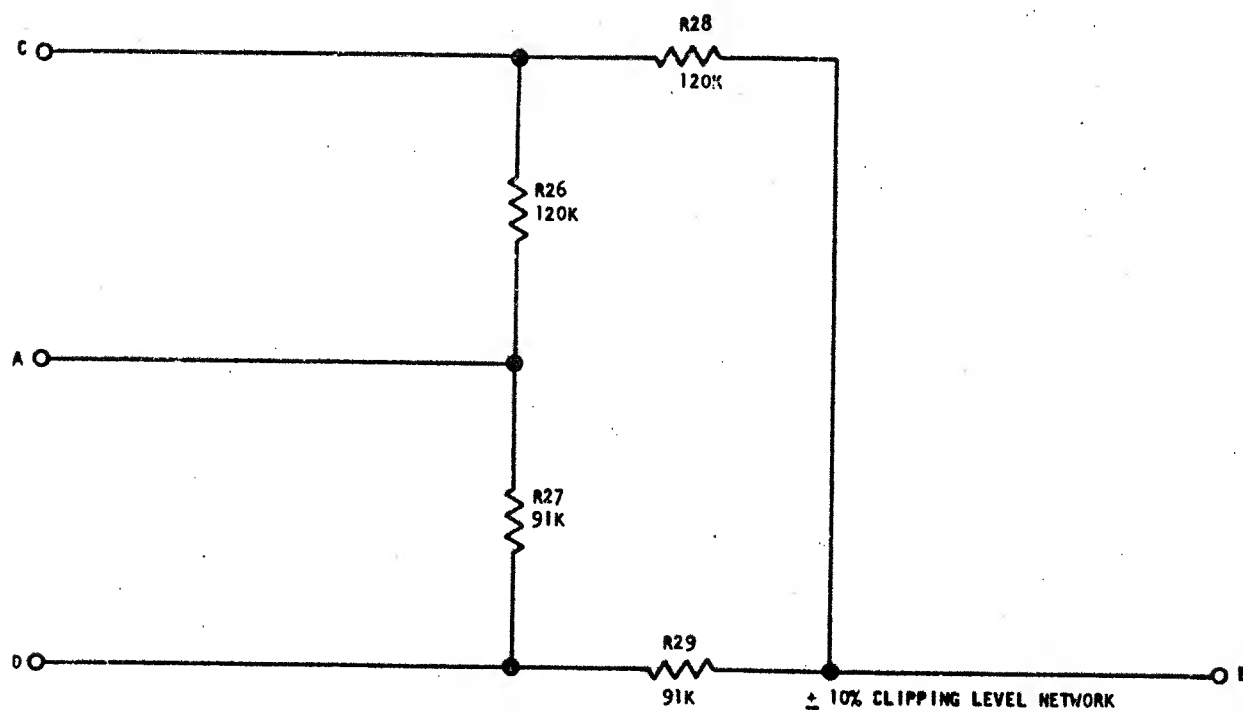
NOTES:

1. SCOPE: TEKTRONIX 561-A WITH 3A1 PREAMP.
2. SYNC: EXTERNAL ON TRACK START WITH DELAYED SWEEP.
3. DISPLAY: TRACES NO. 1 THROUGH 8, LAST BITS OF AGC AND FIRST BITS OF ADDRESS: 9 & 10, APPROX. ONE FULL SECTOR.

MARGINAL CLIP & X10 AMPLIFIER C.E.

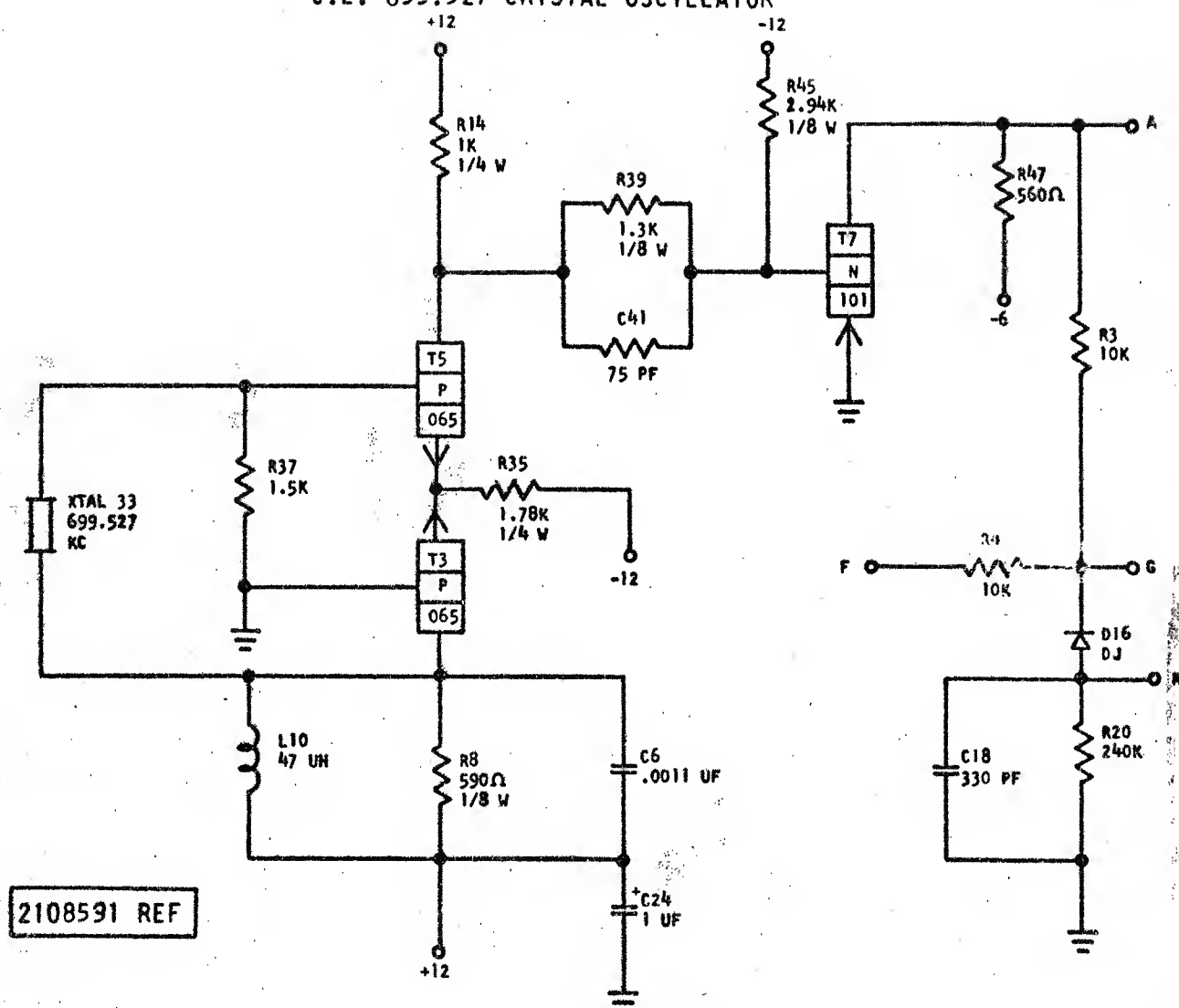


2108594 REF

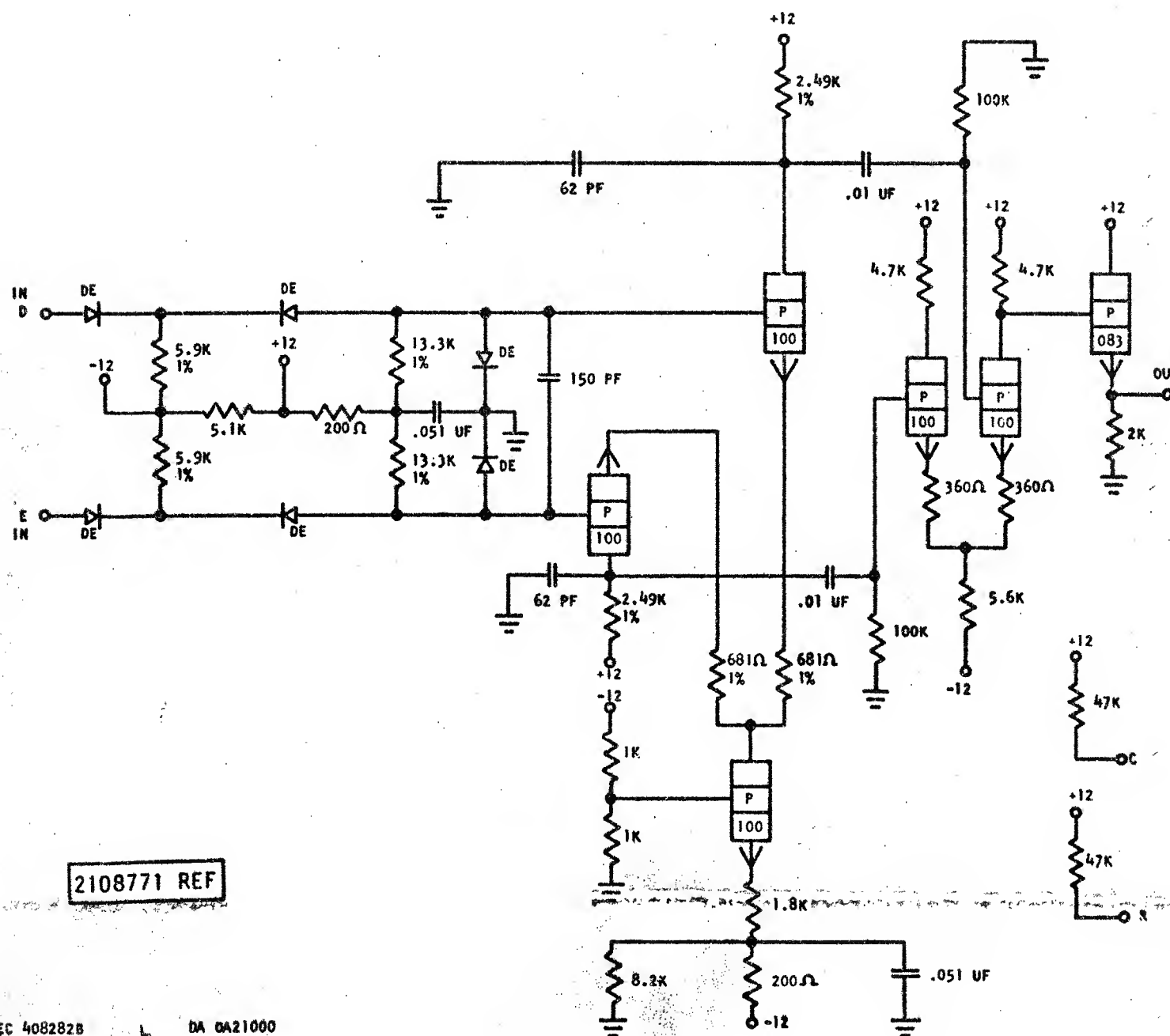
MARGINAL CLIP
C.E.

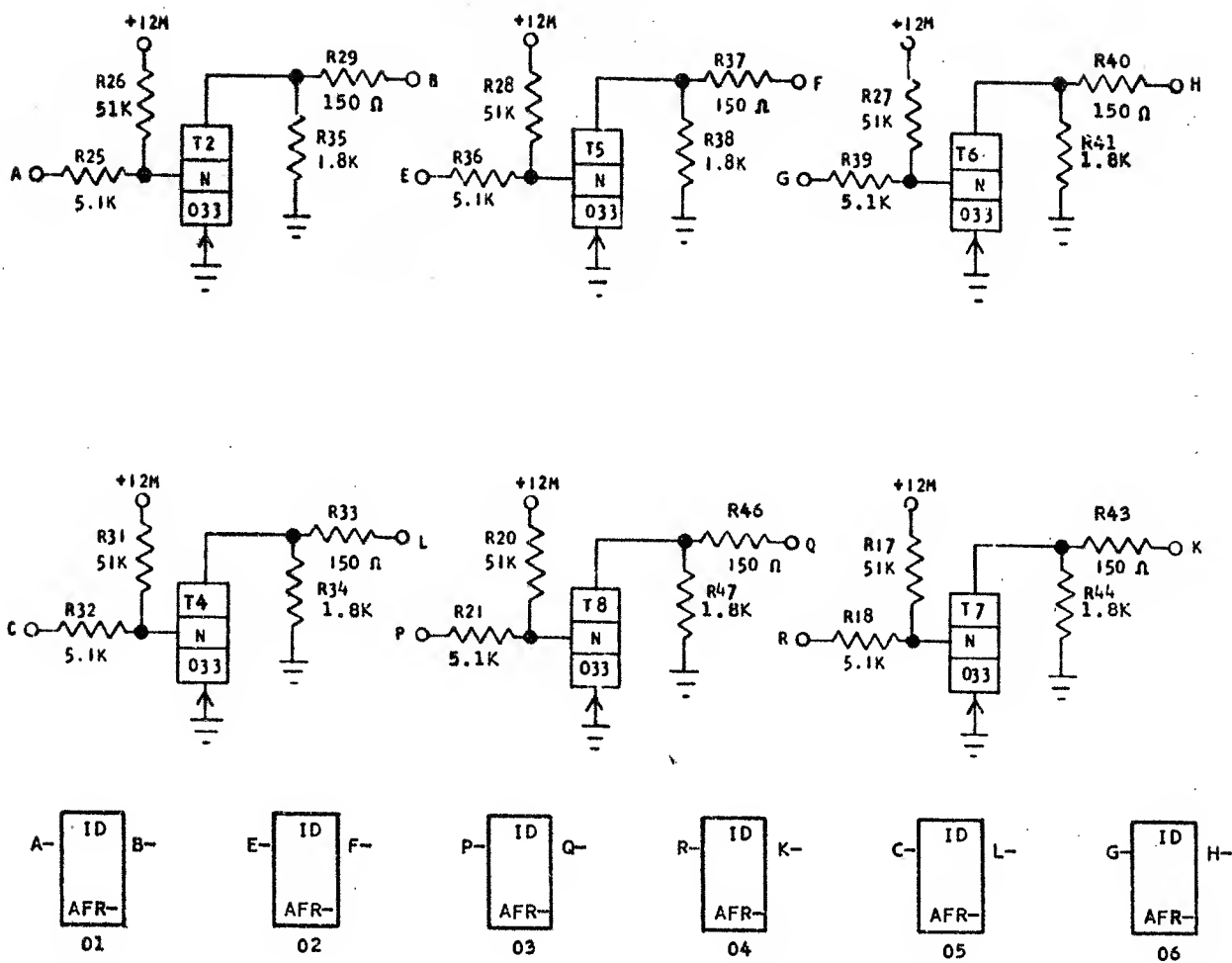
2108770 REF

C.E. 699.527 CRYSTAL OSCILLATOR



C.E. X20 AMPLIFIER

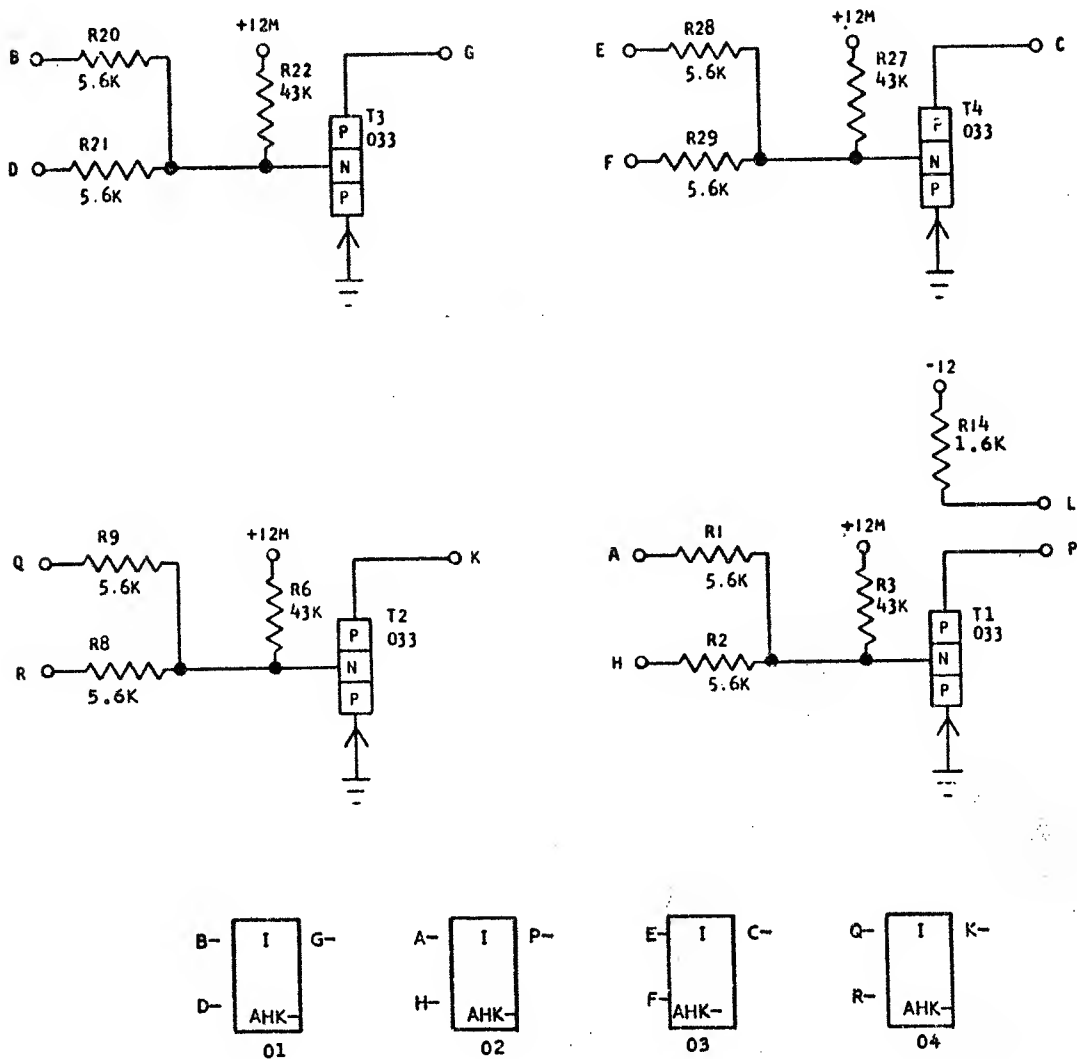




371943 REF

CTRL - INVERTER "N" 2 WAY EXTENDER

AHK

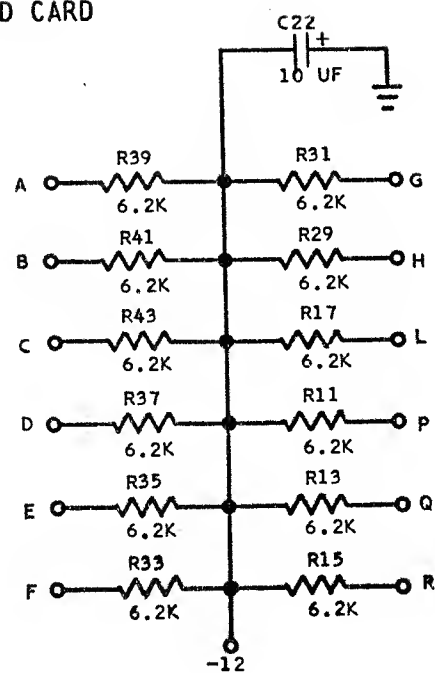


370322 REF

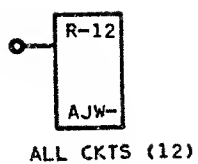
E/C 407002 7-5-62

DA 0A00000

6.2K LOAD CARD

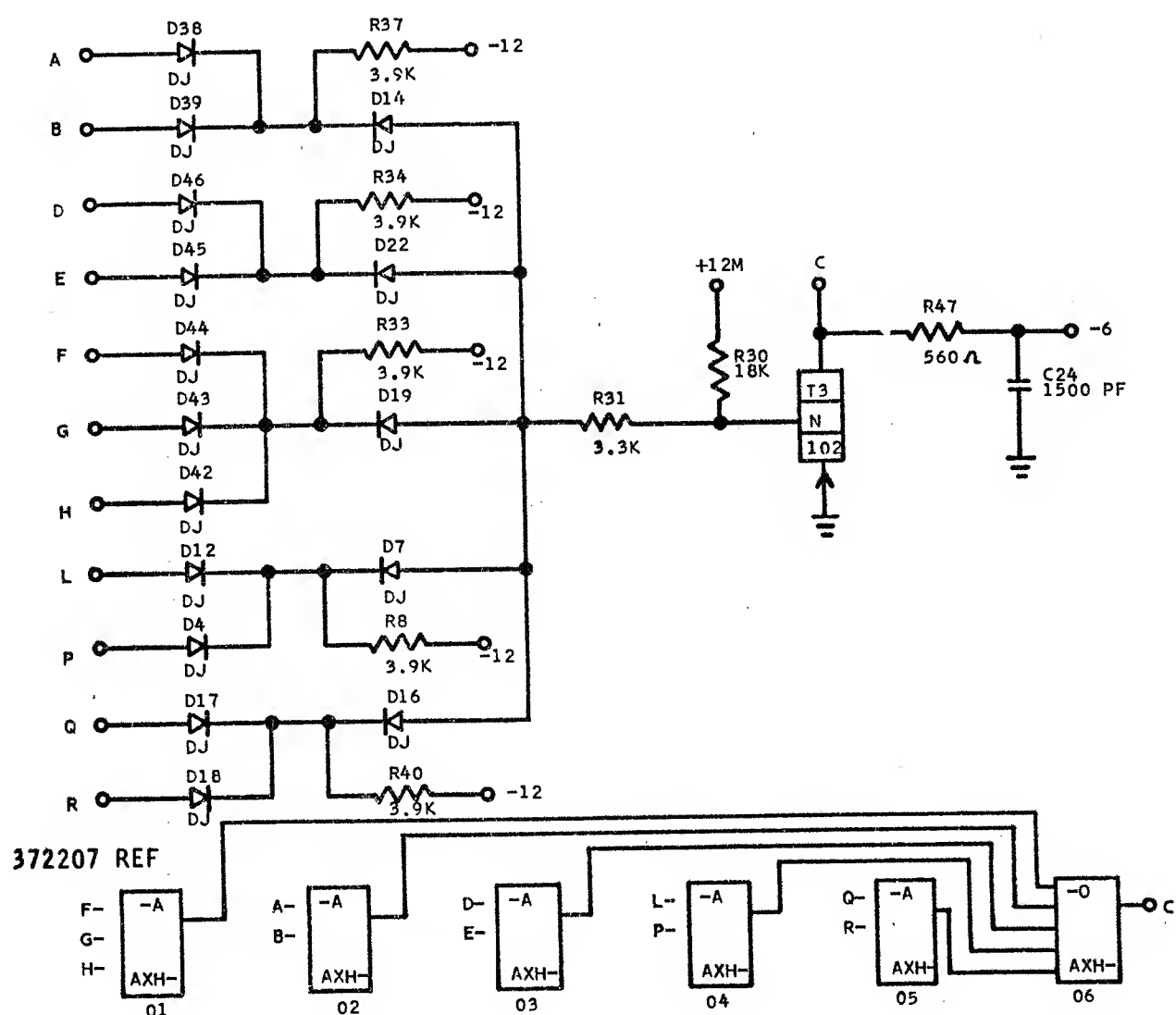


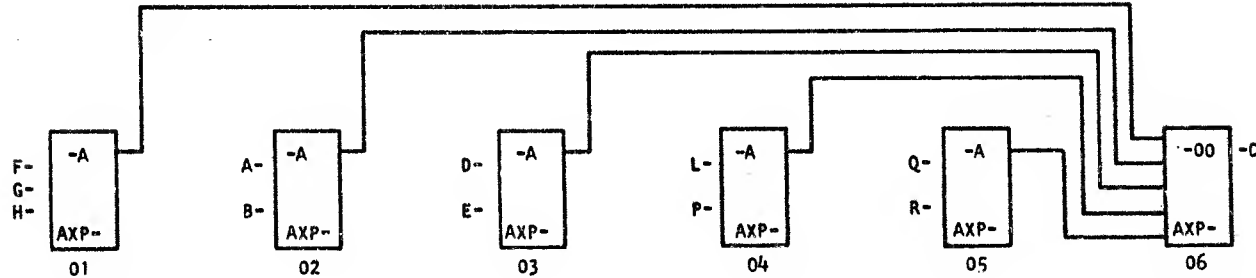
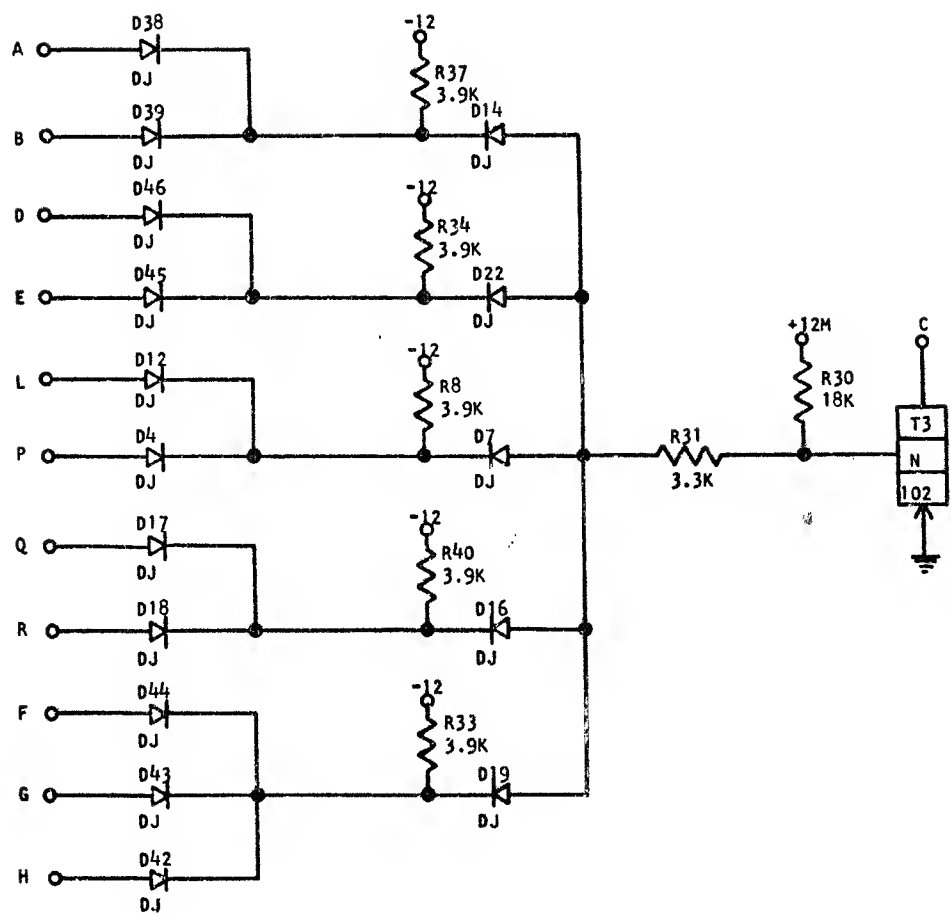
370643 REF



4-2 WAY, 1-3 WAY (-A,-0)

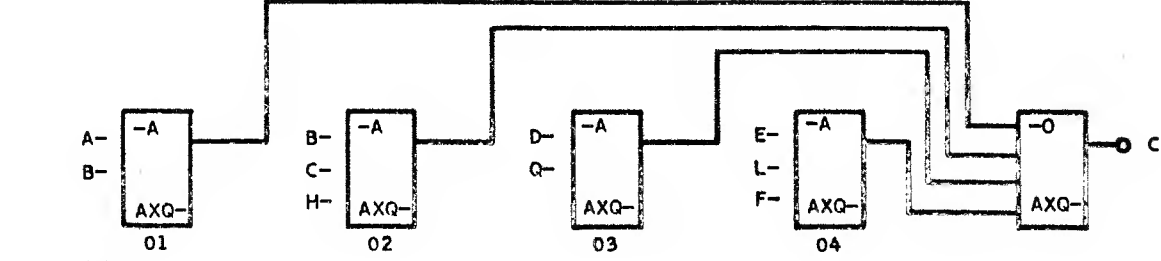
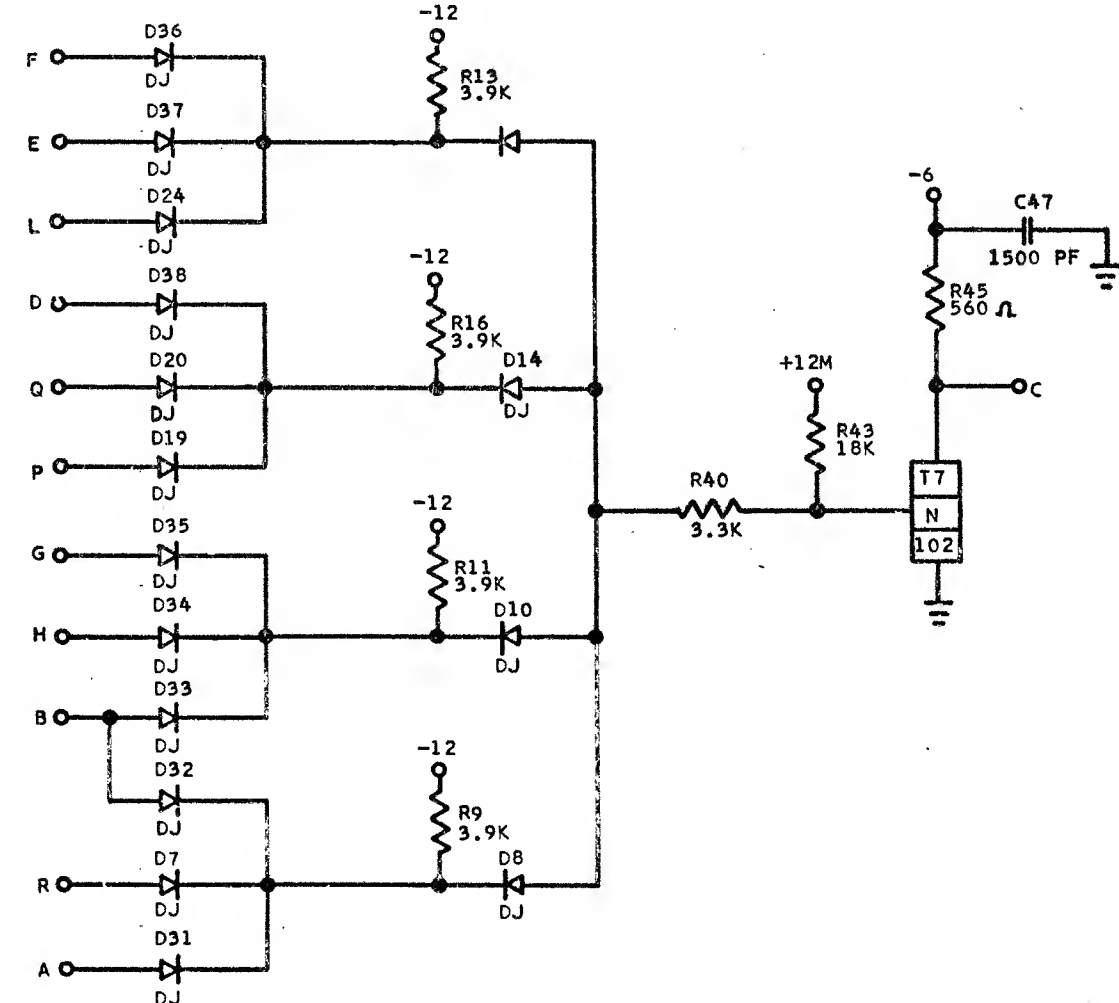
AXH-





372213 REF.

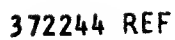
SDTDL 4 - 3 WAY (-A,-O) W/LOAD



372214 REF

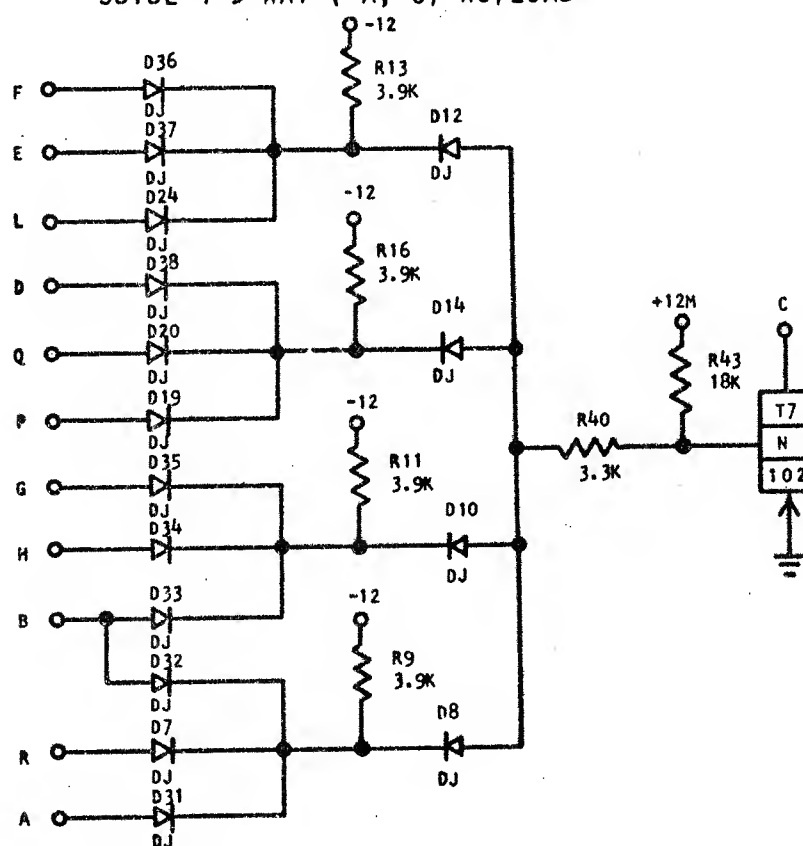
COMPLEMENTARY EMITTER FOLLOWER

AXV-

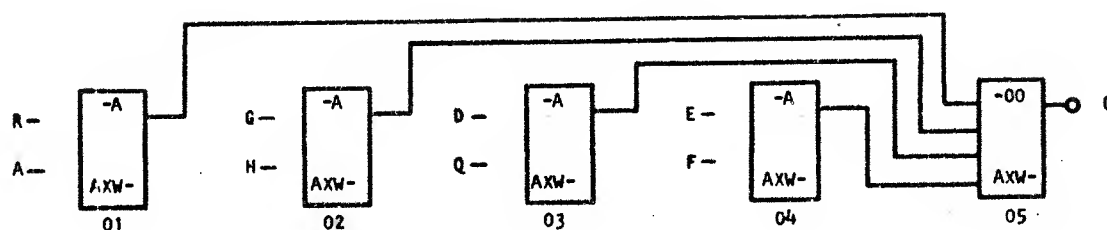


SDTDL 4-3 WAY (-A,-O) WO/LOAD

AXW-

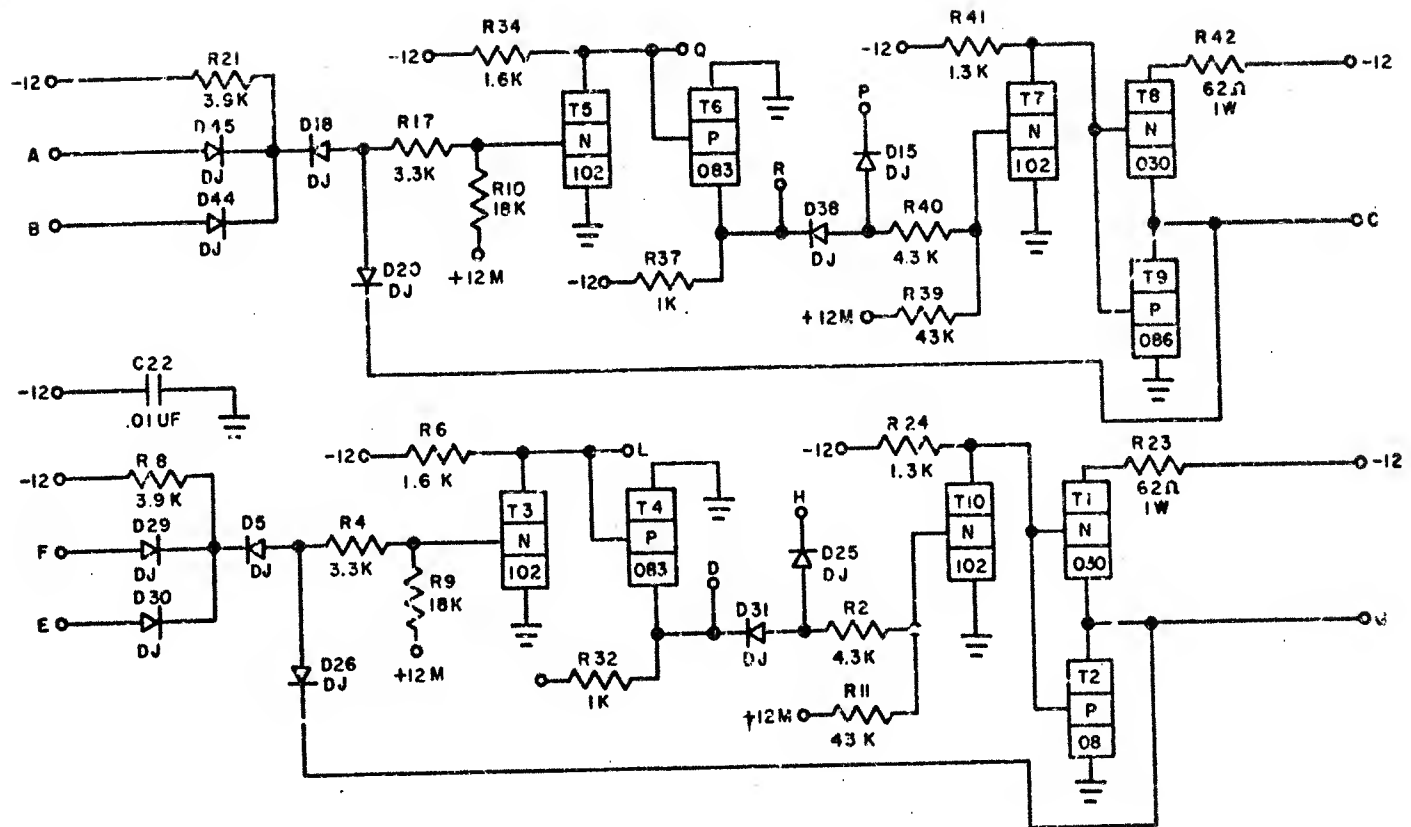


372236 REF

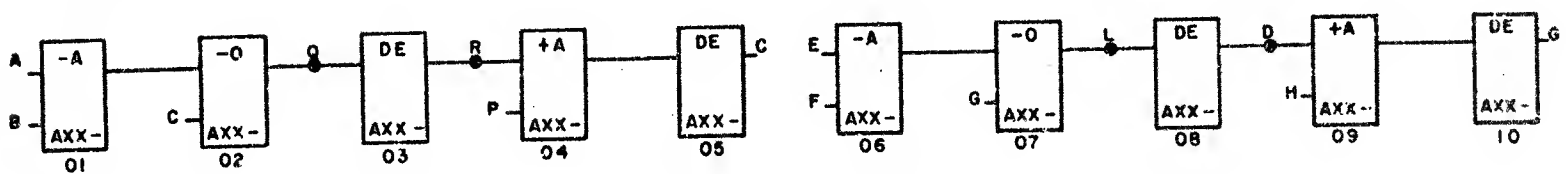


SDTDL POWER LATCH A

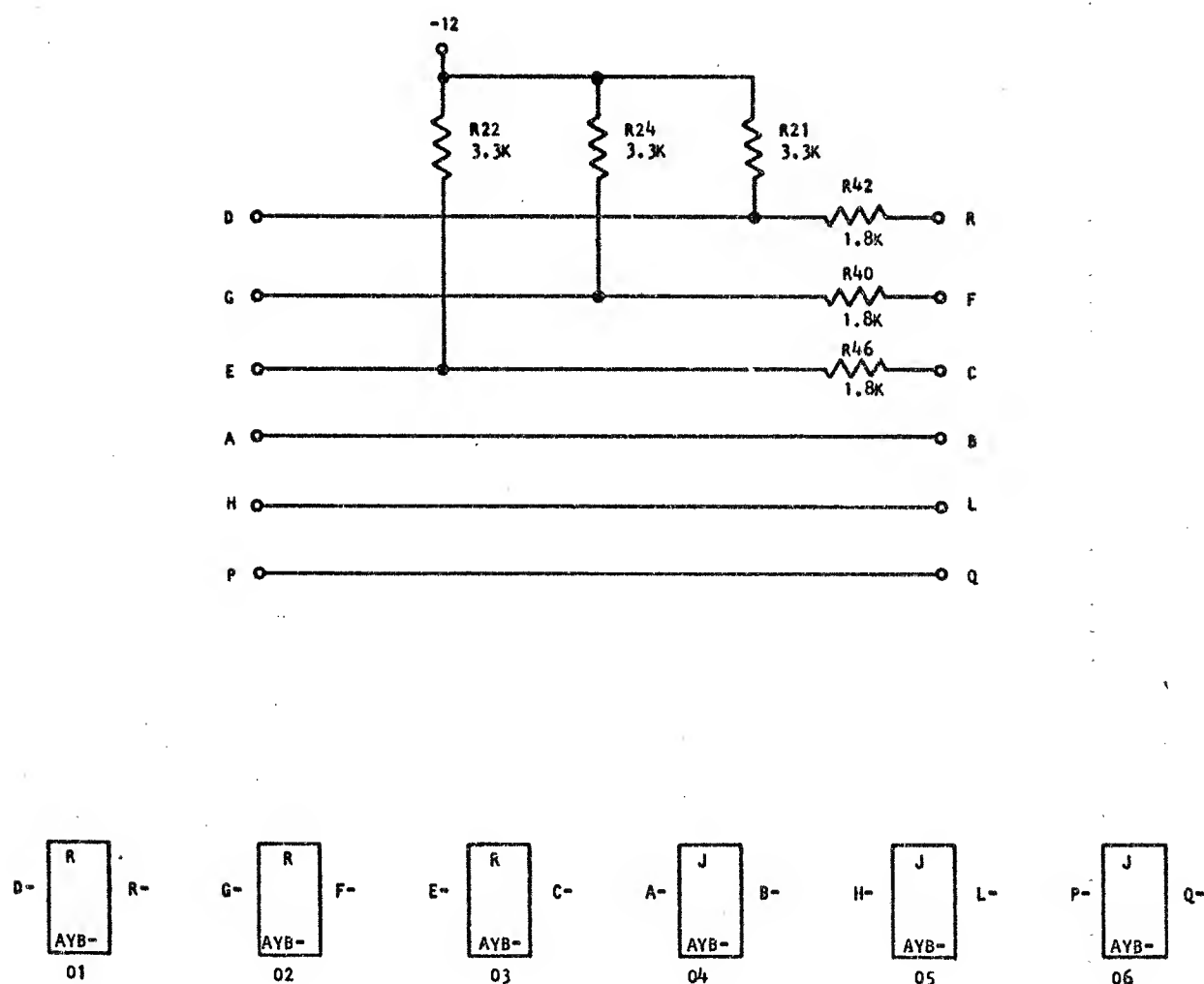
AXX-



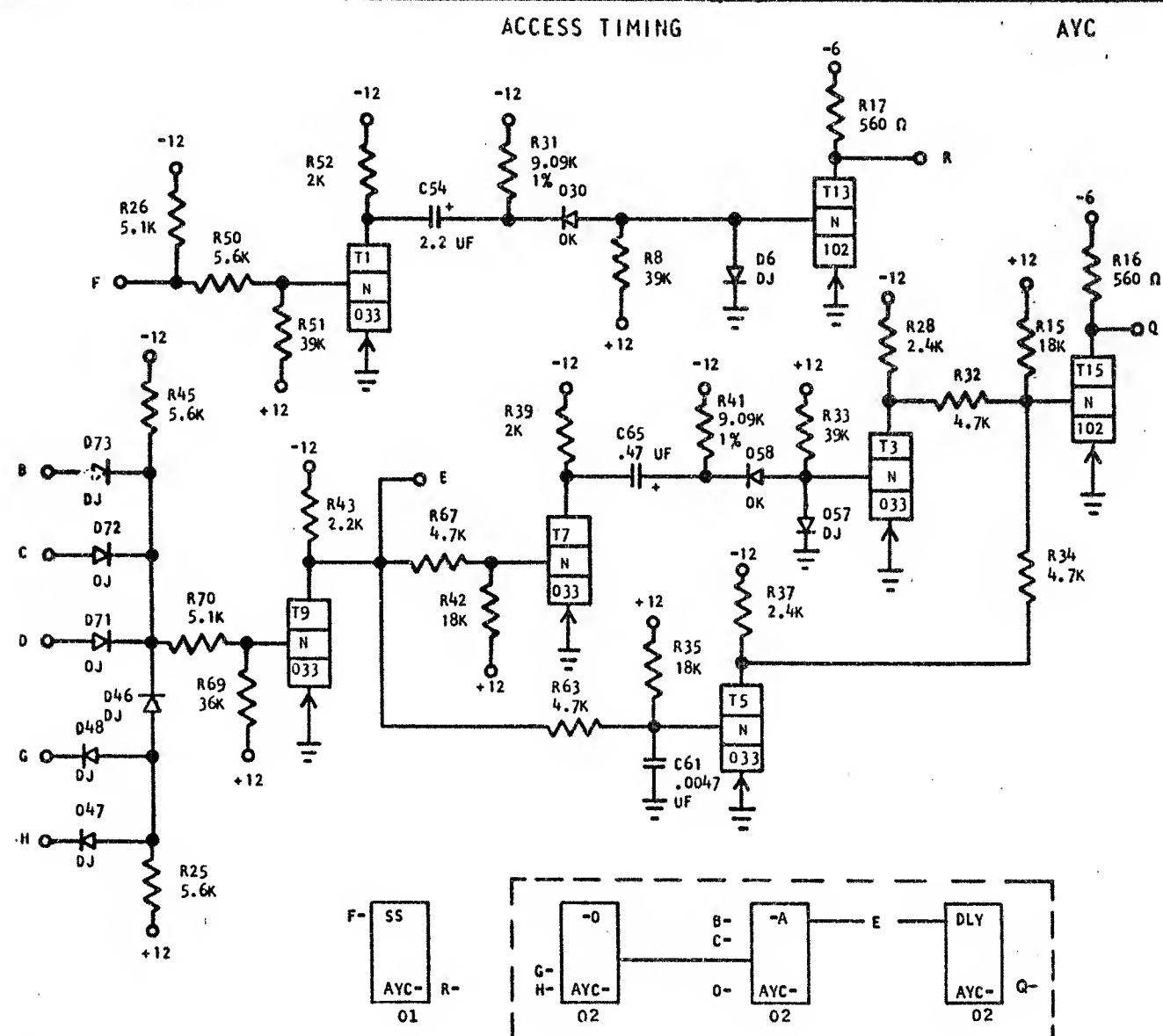
372237 REF



AYB



372316 REF



372311 REF

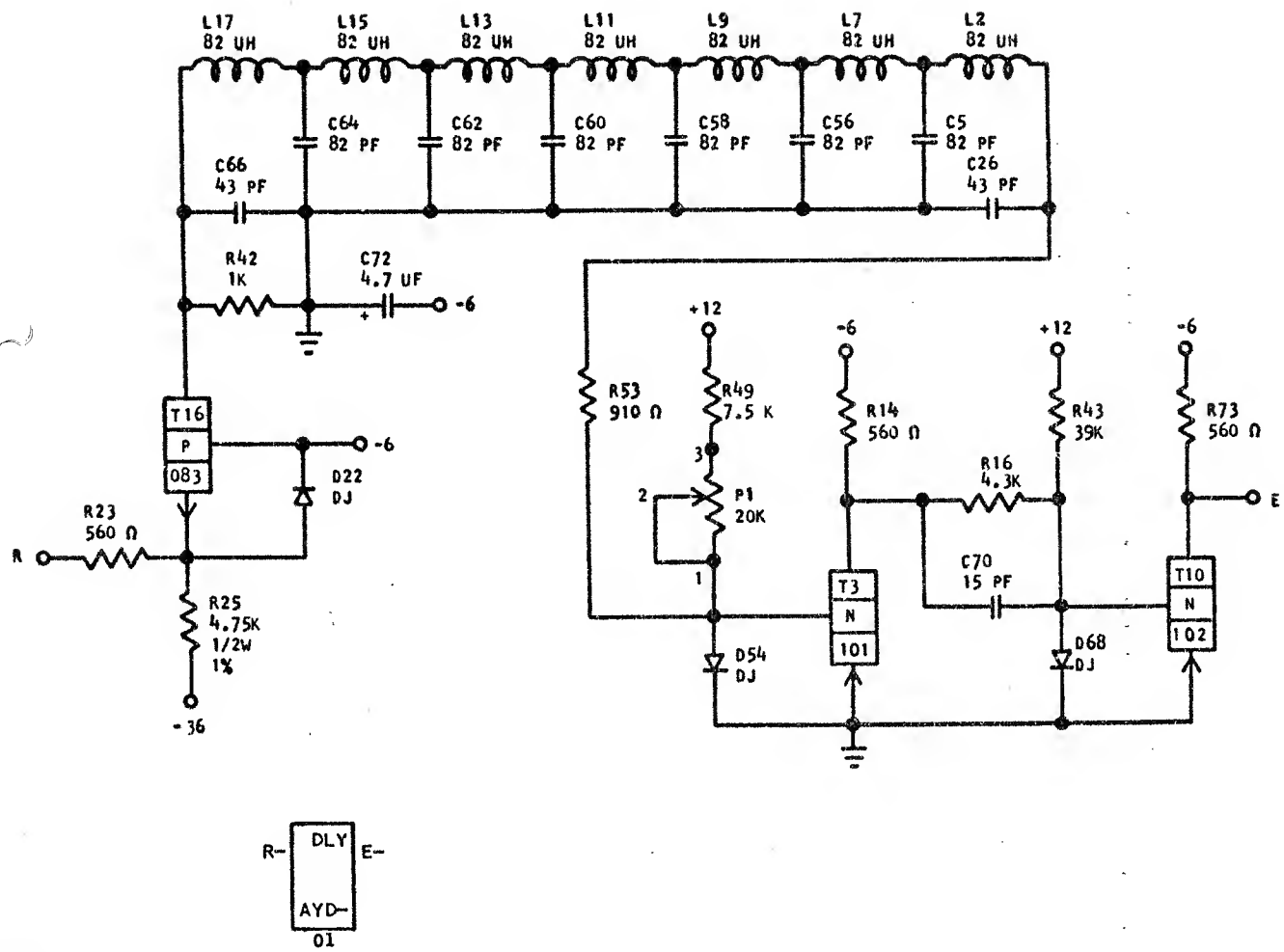
2157202

.75 US DELAY CIRCUIT

1311

C2.90.02.0

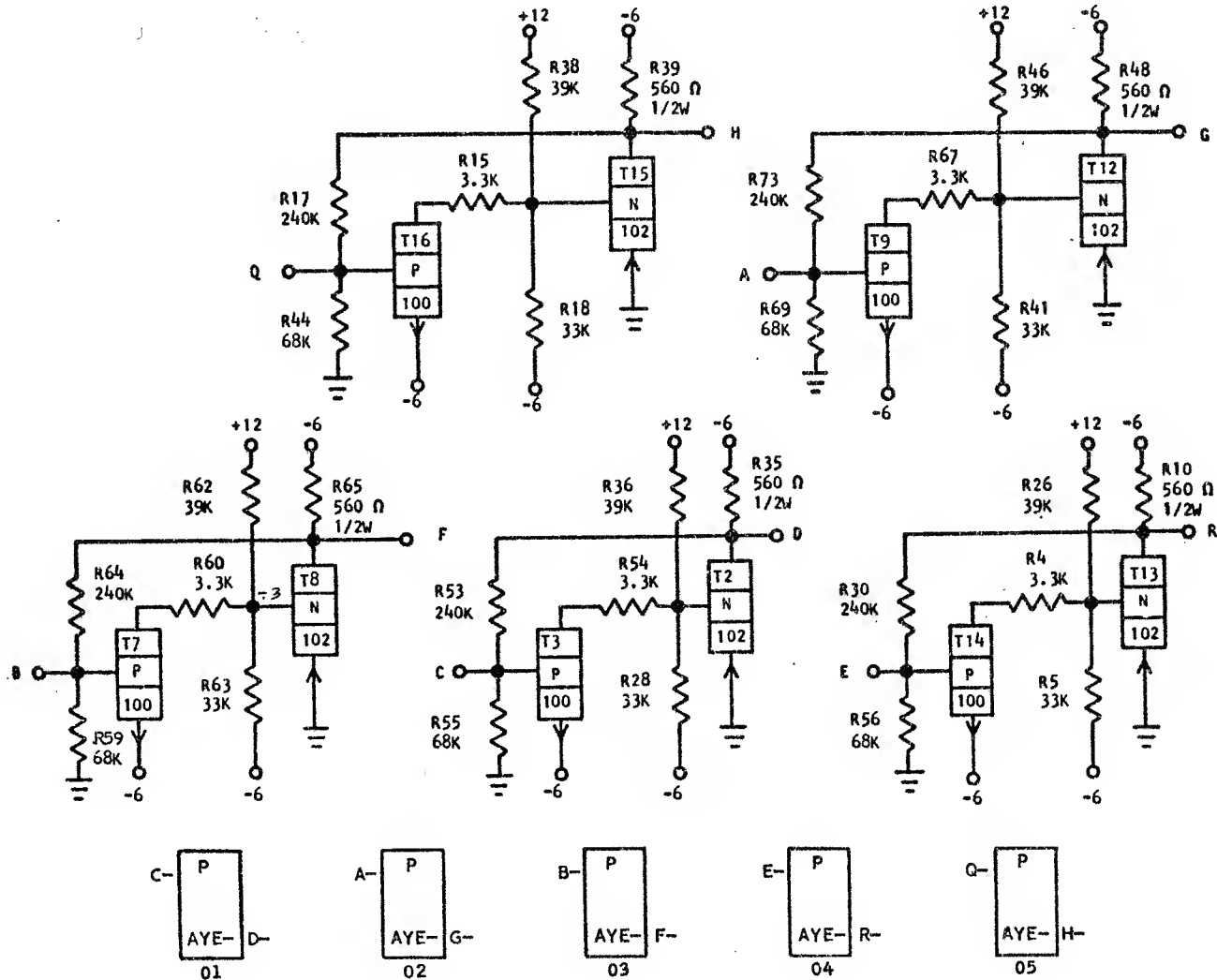
AYD



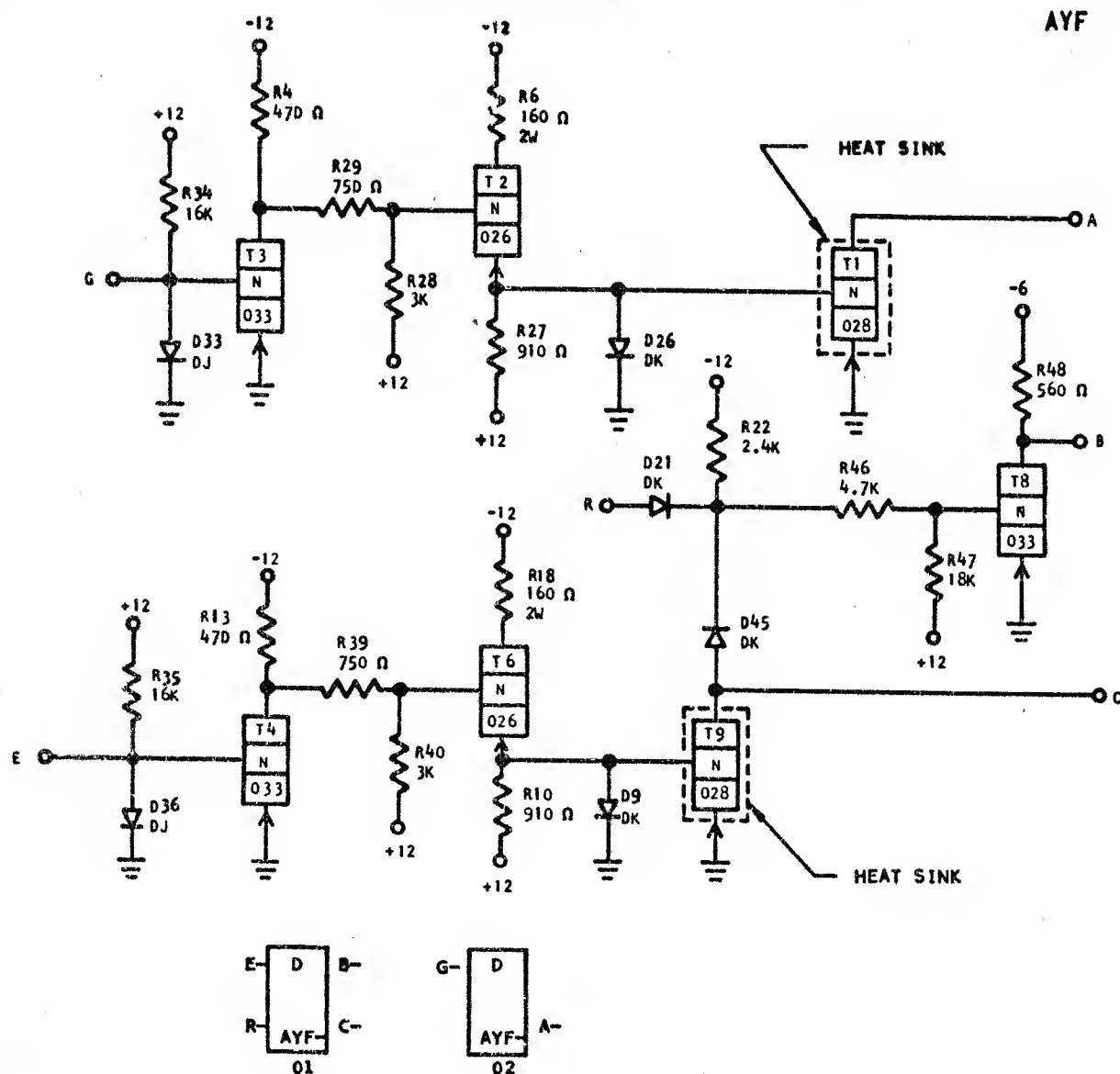
372305 REF

PHOTO CELL AMPLIFIER

AYE



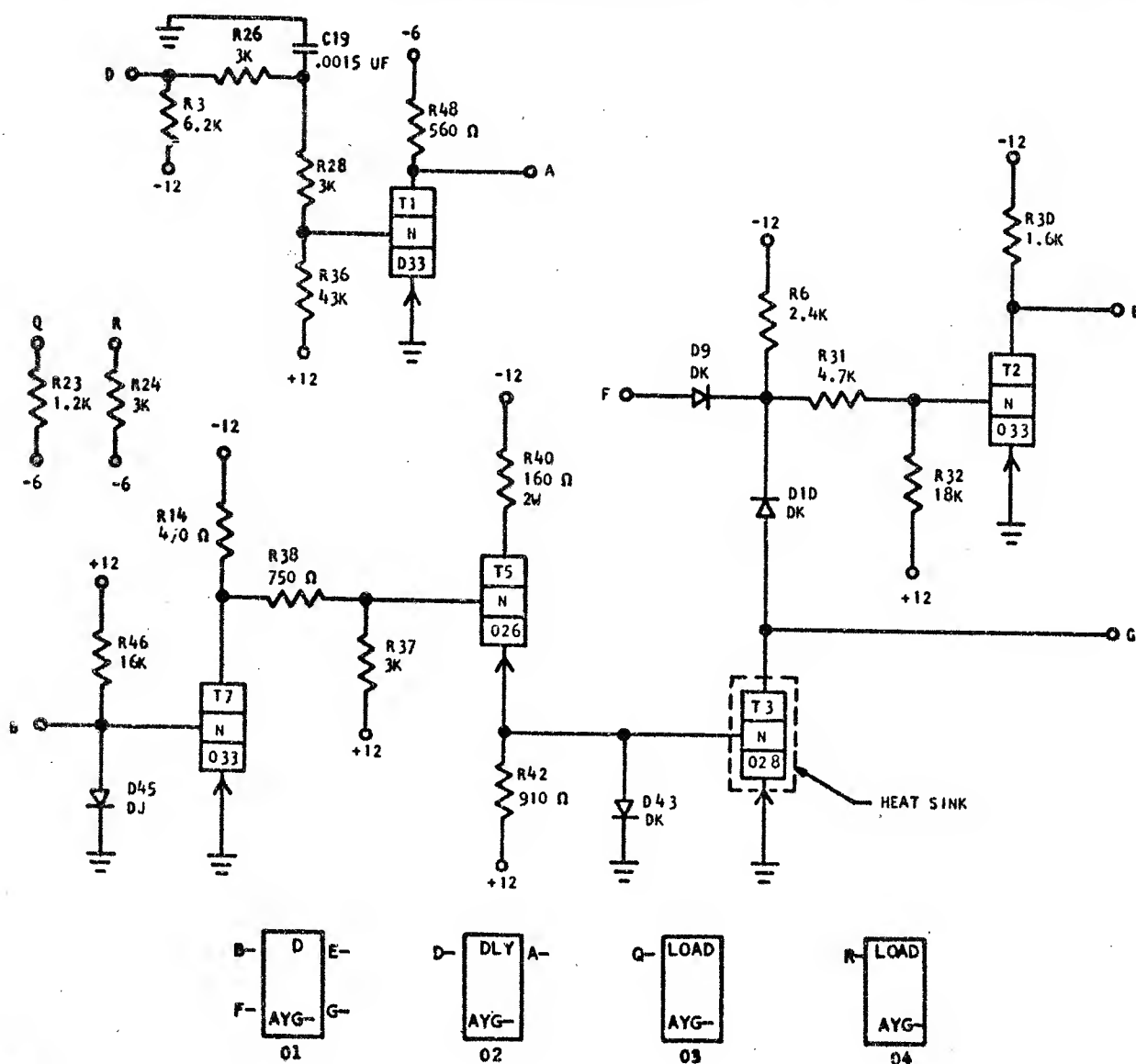
372298 REF



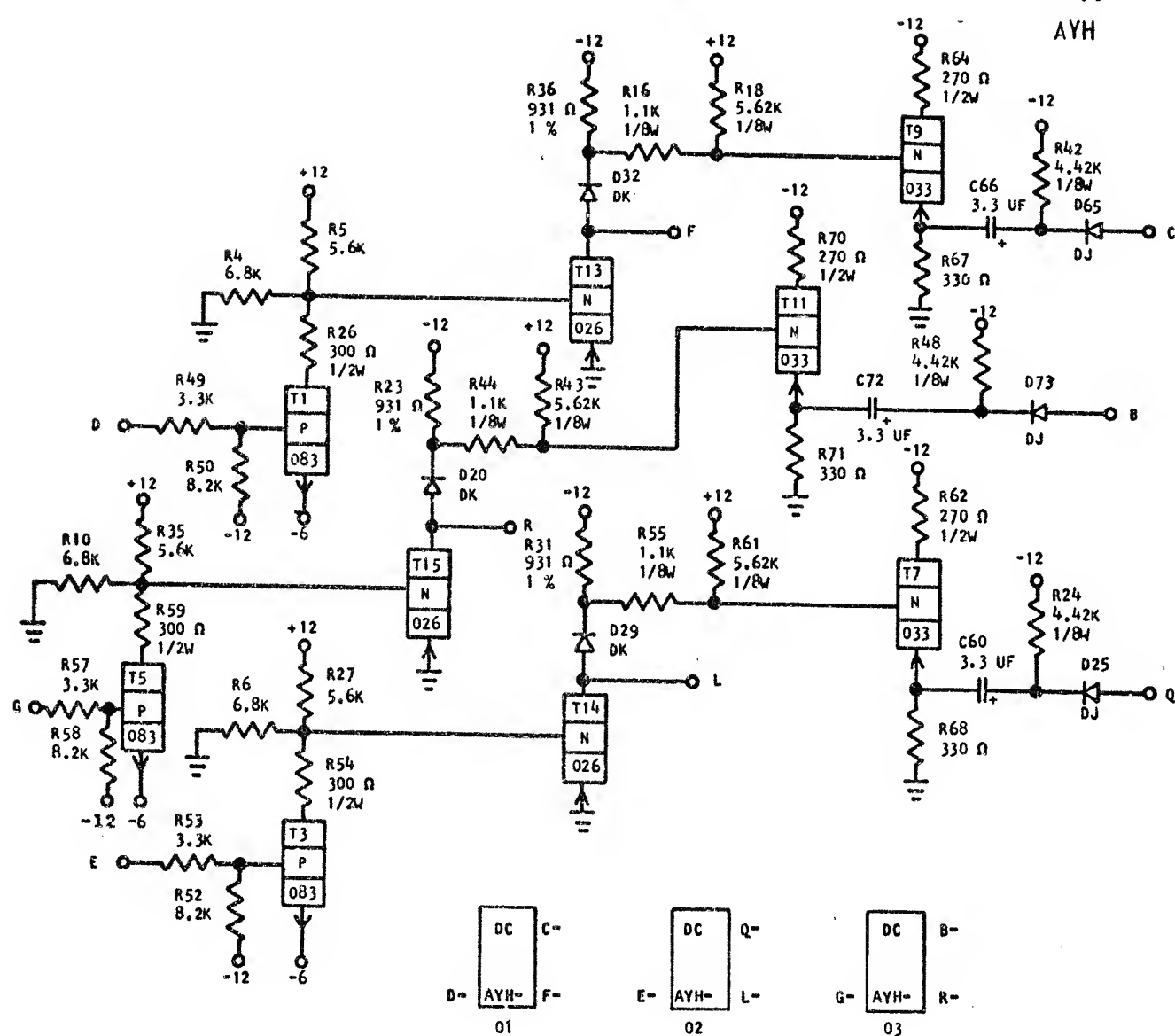
372313 REF

SOLENOID DRIVER NO.2

AYG



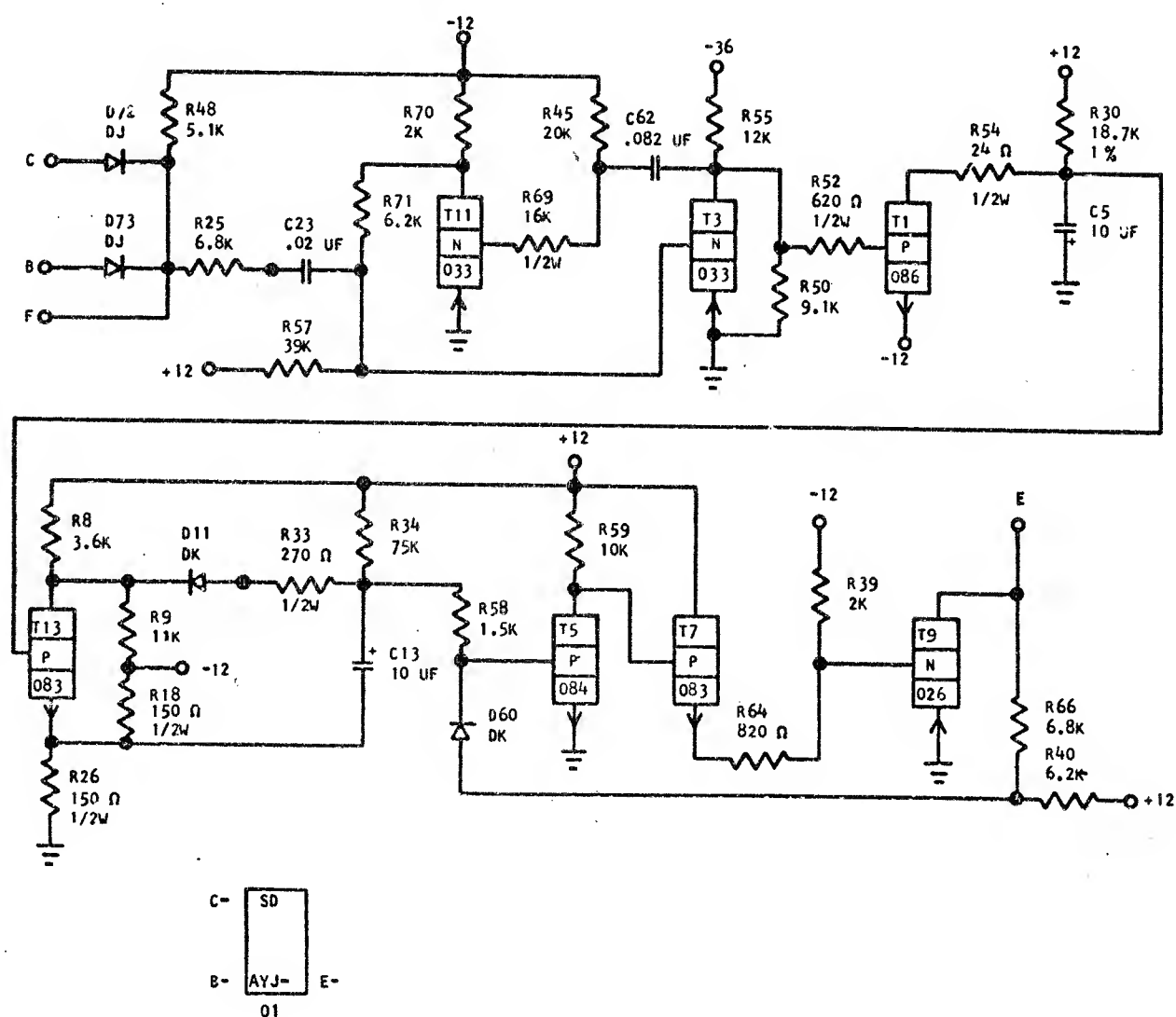
372314 REF



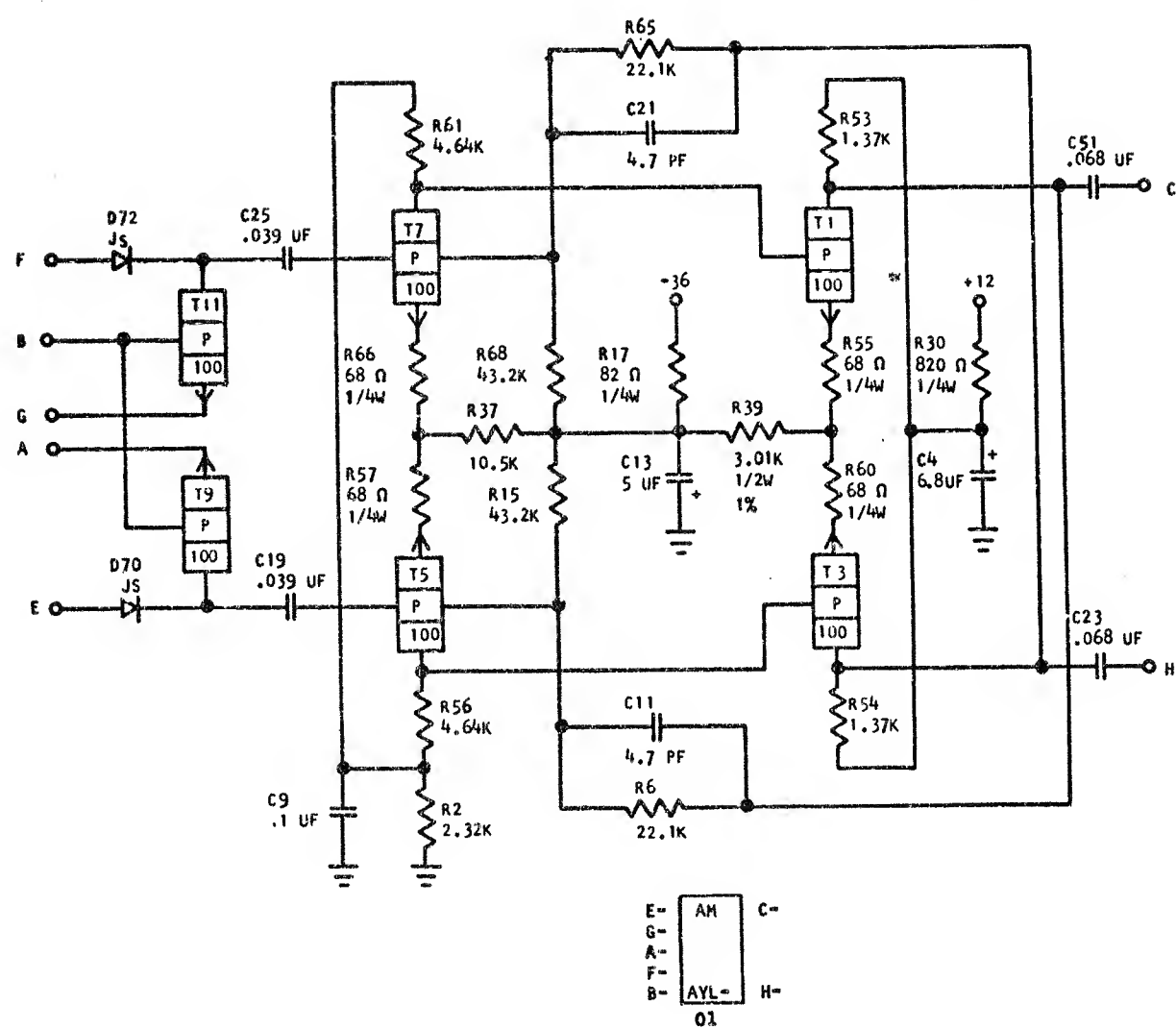
372315 REF

DISK SPEED DETECTOR

AYJ



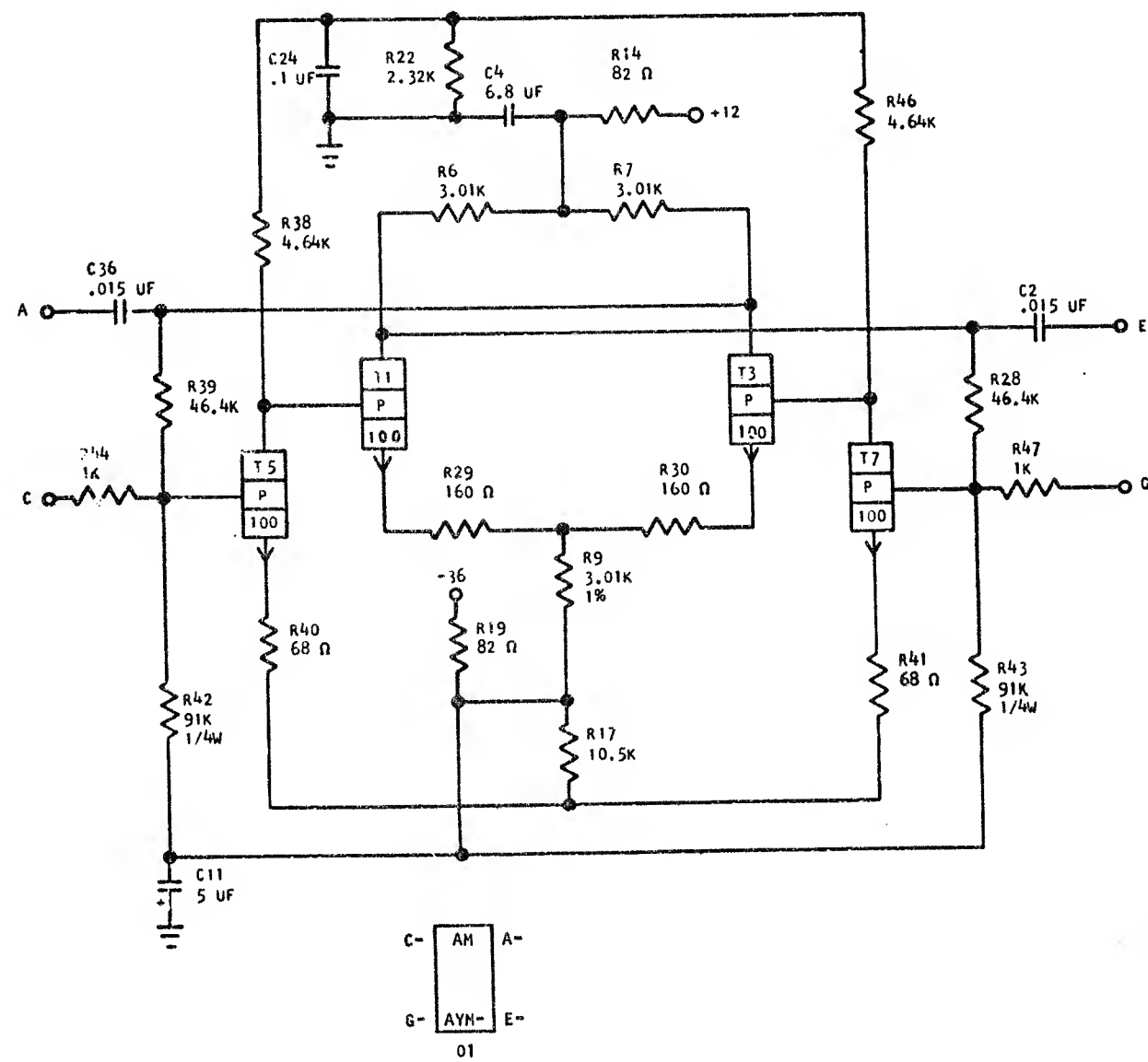
372296 REF



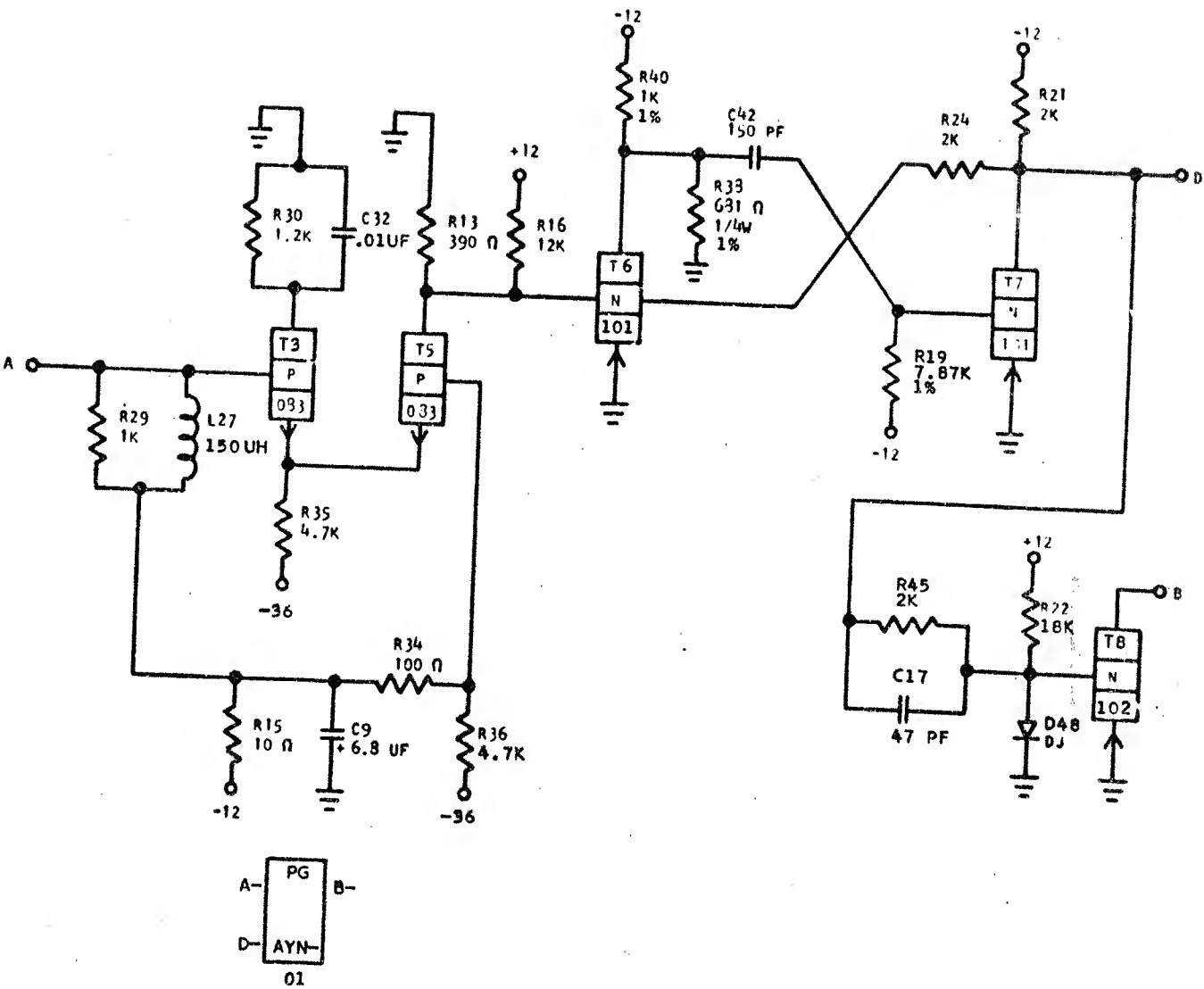
372301 REF

HIGH LEVEL AMPLIFIER

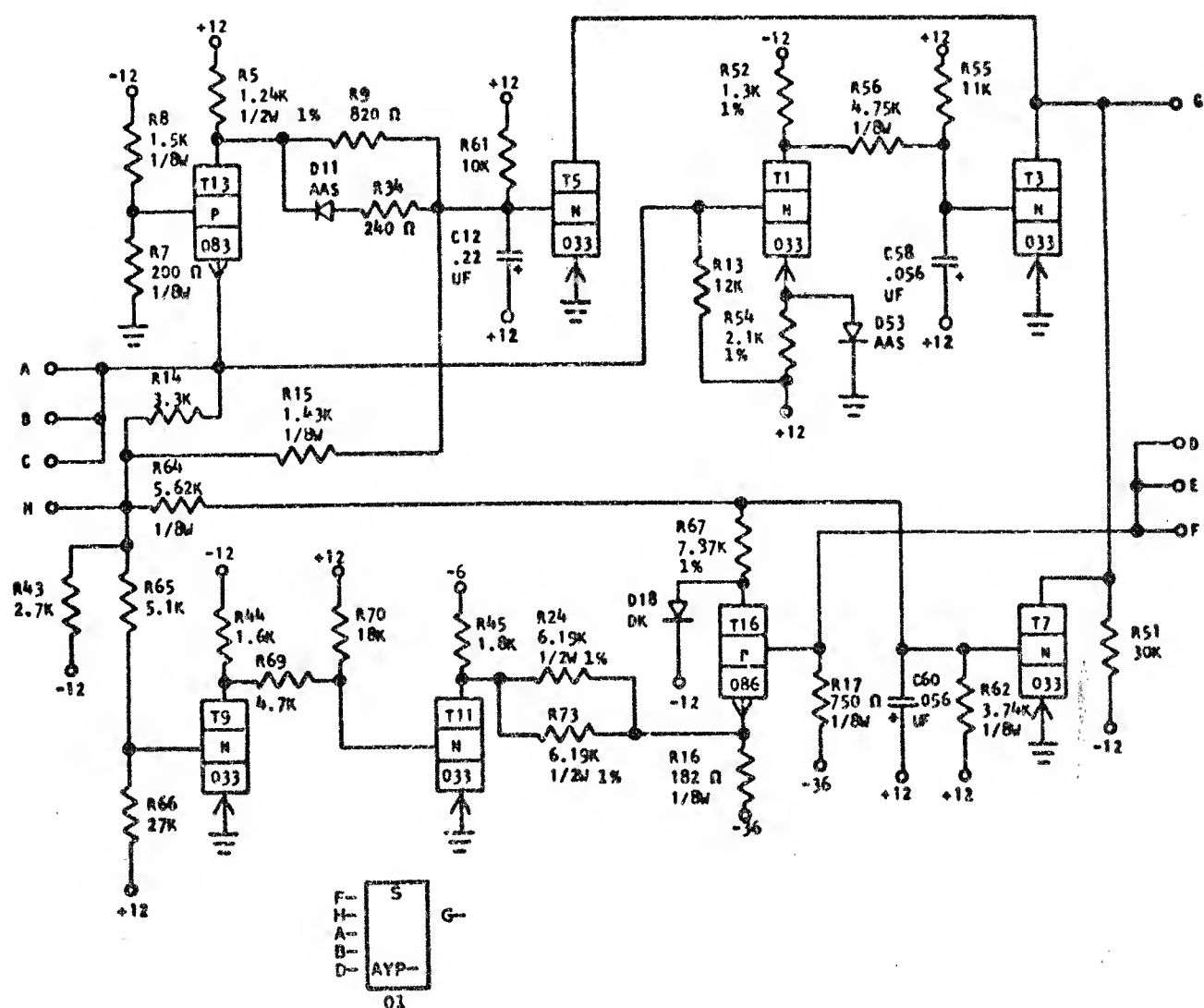
AYM



372302 REF



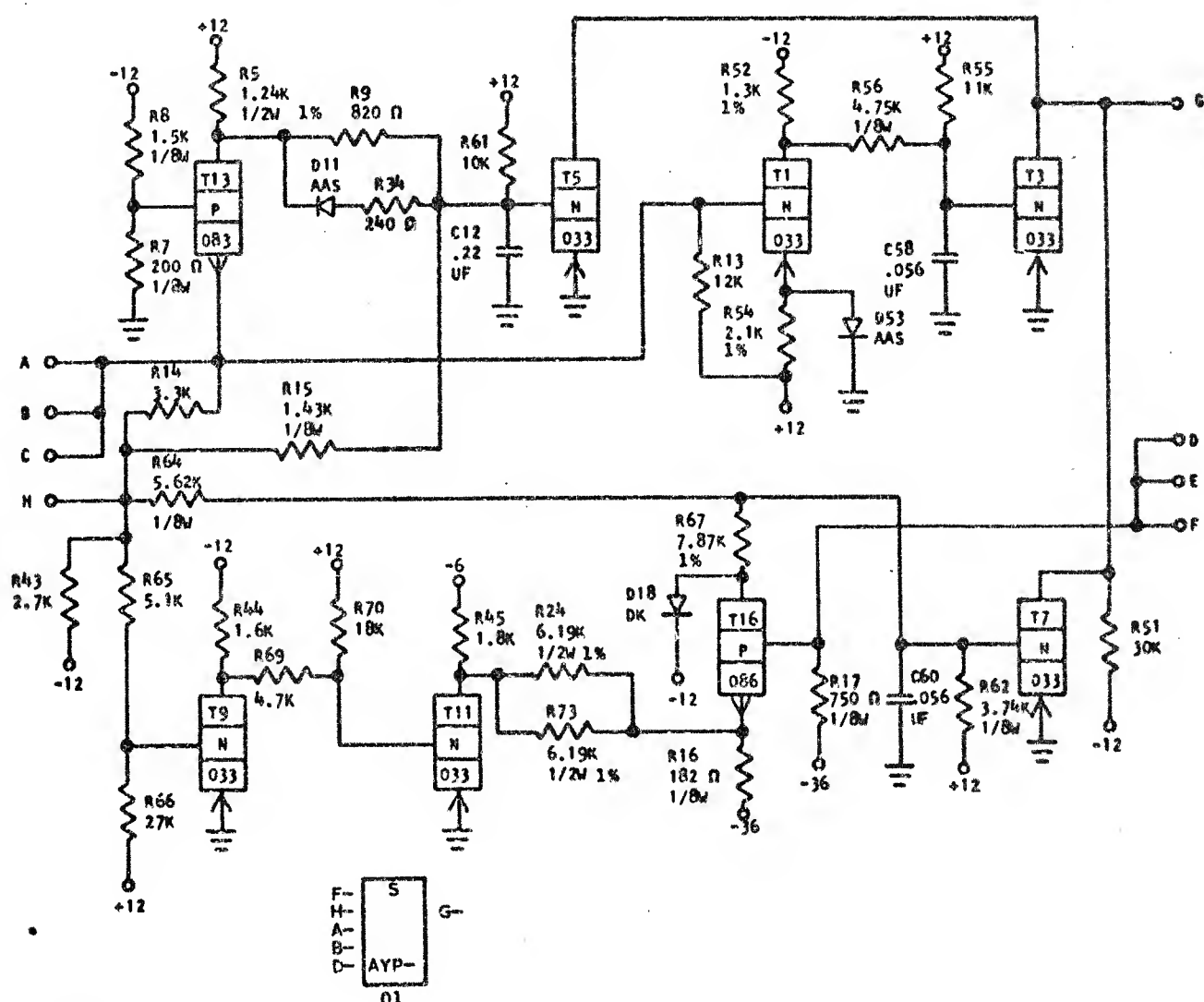
372303 REF



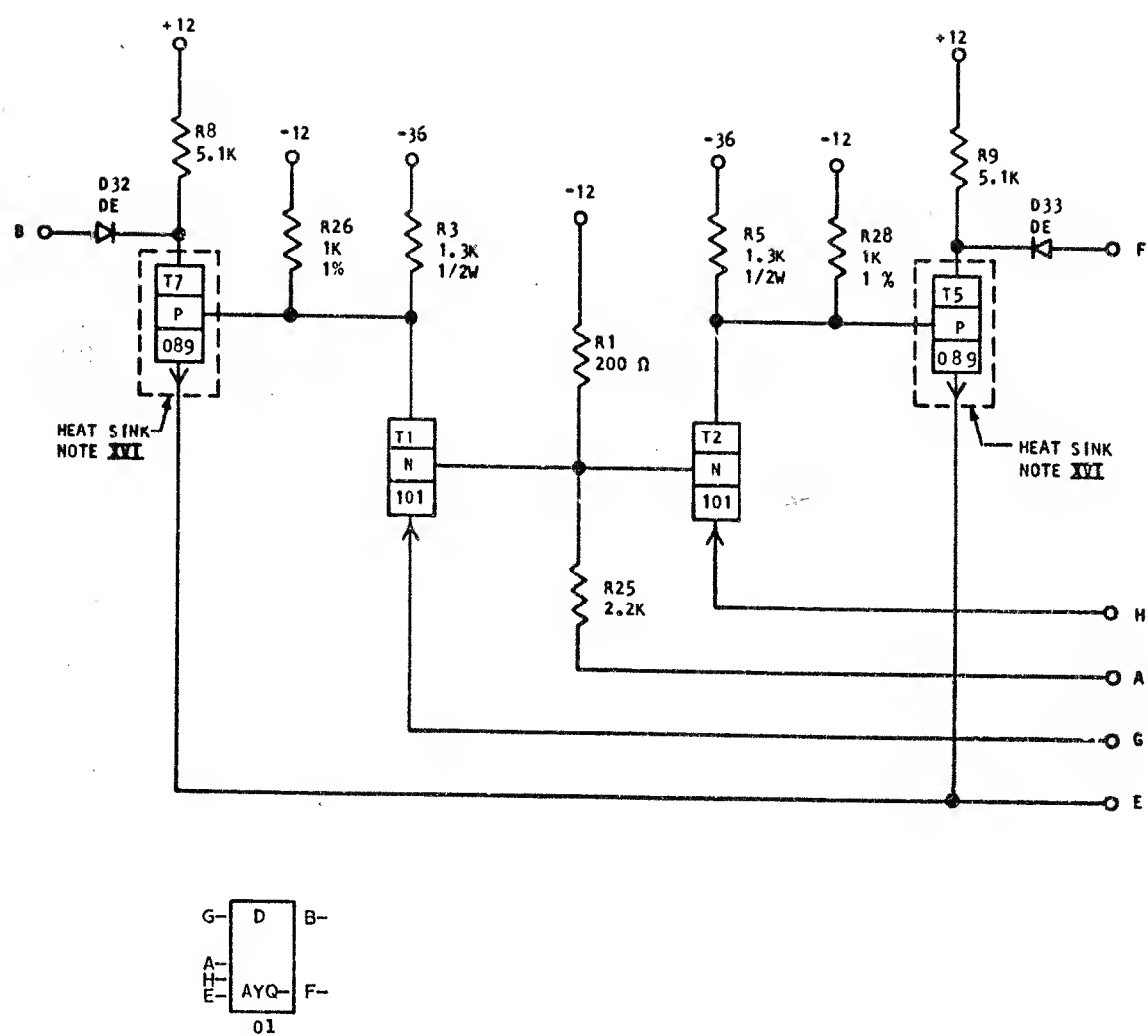
372308 REF EC 113589

WRITE AND ERASE SAFETY

AYP



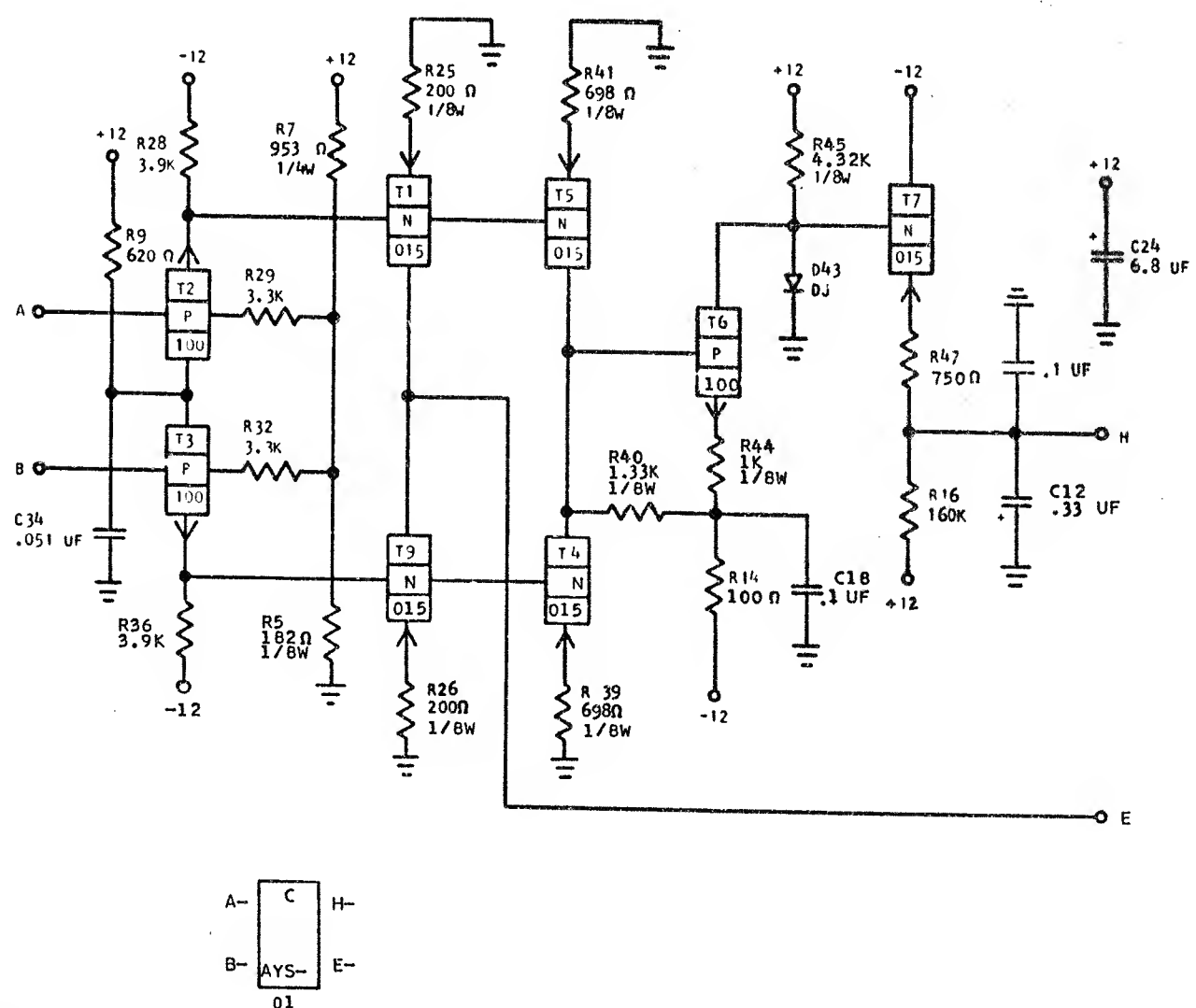
372308 REF EC 117875



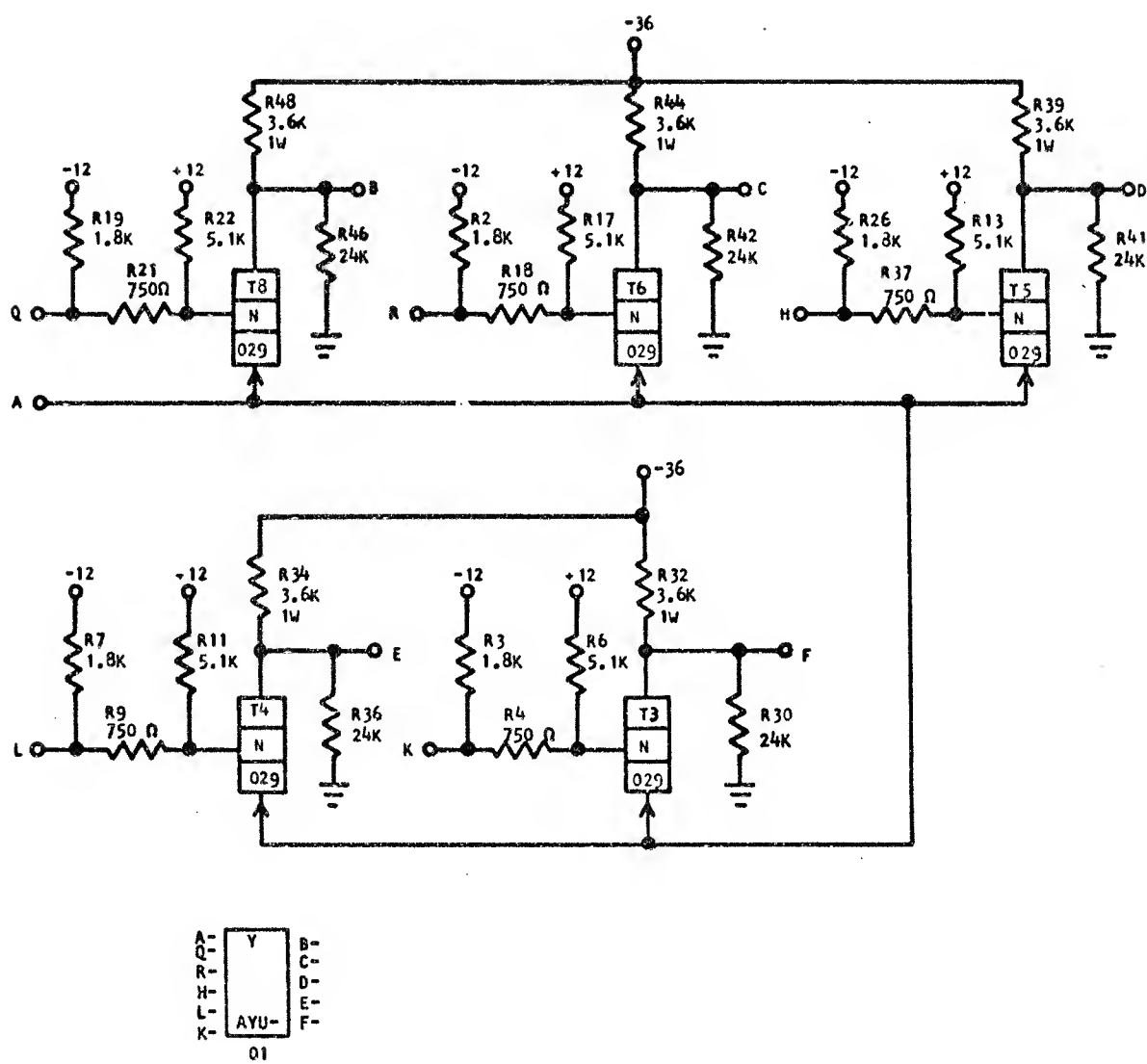
372309 REF

BASE CLIPPER

AYS



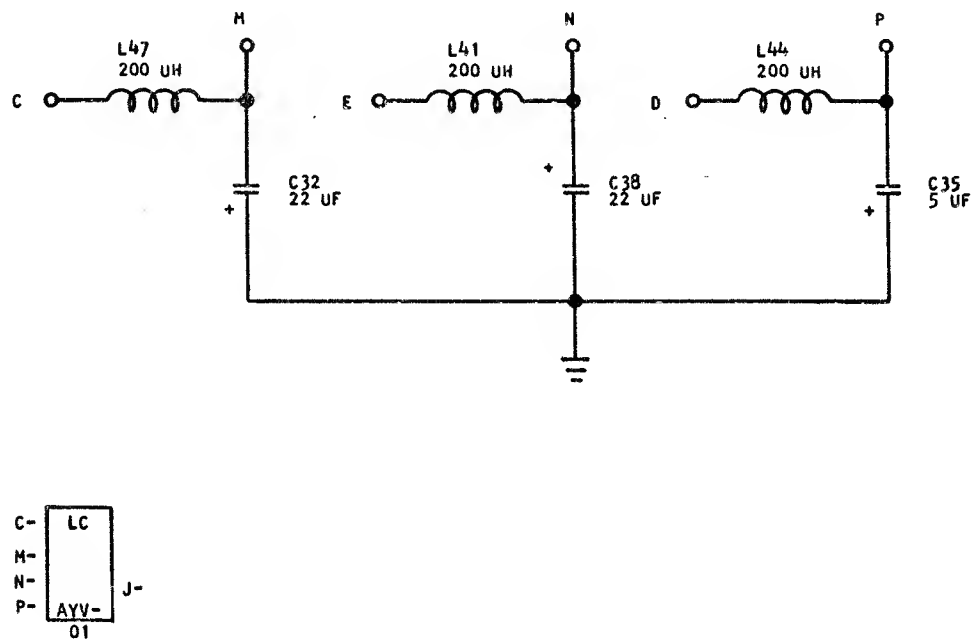
372297 REF



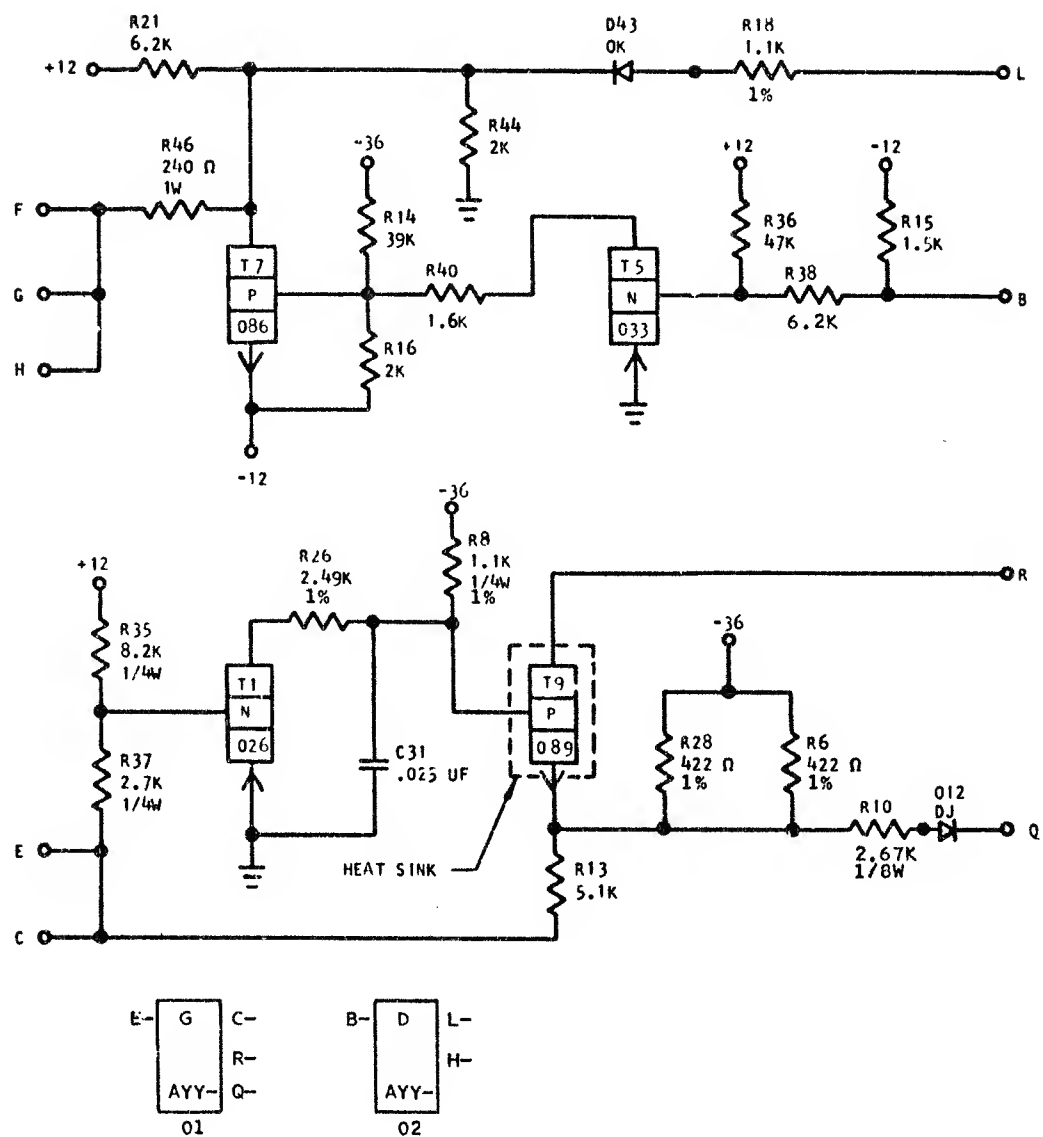
372318 REF

FILTER

AYV



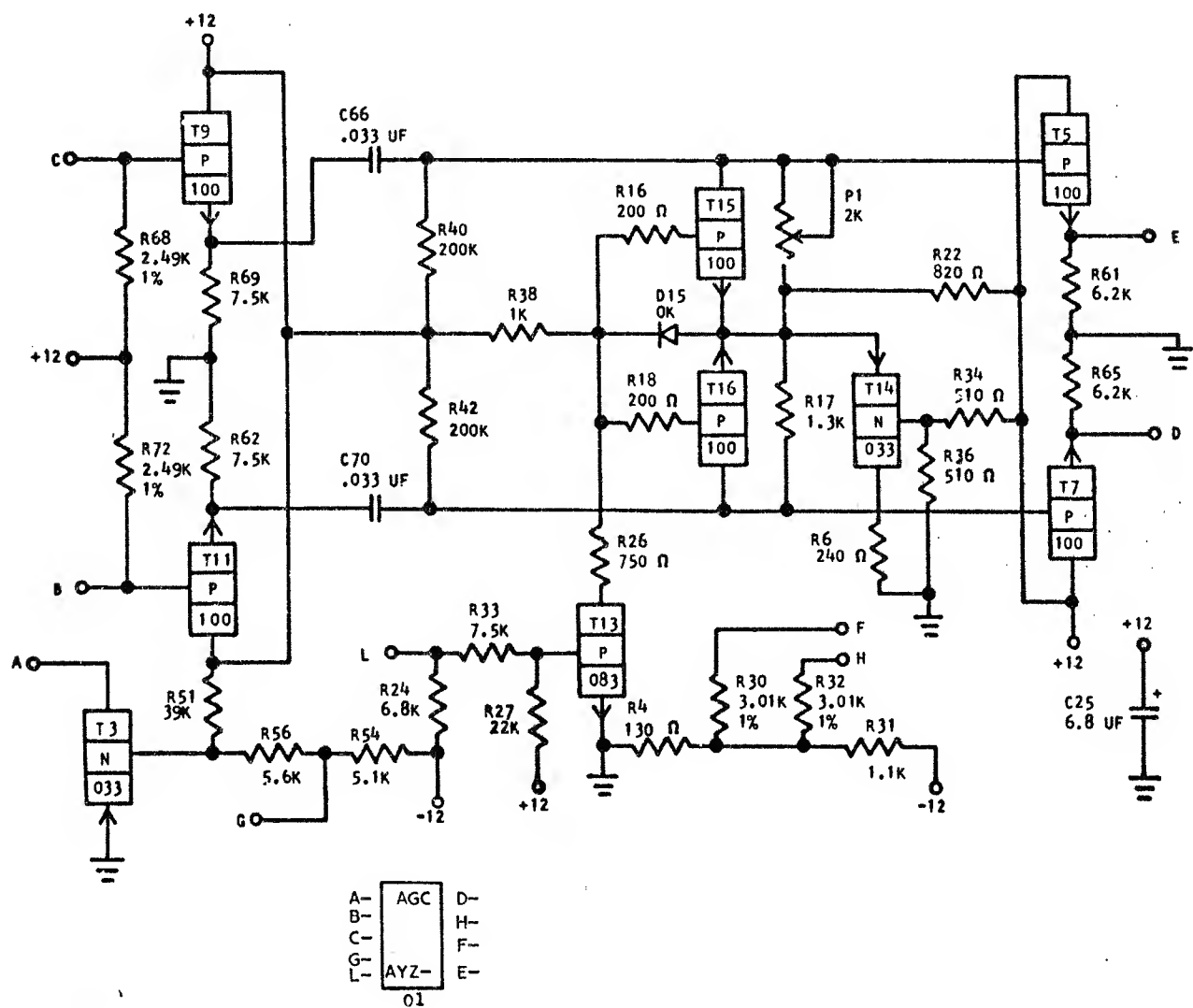
372319 REF



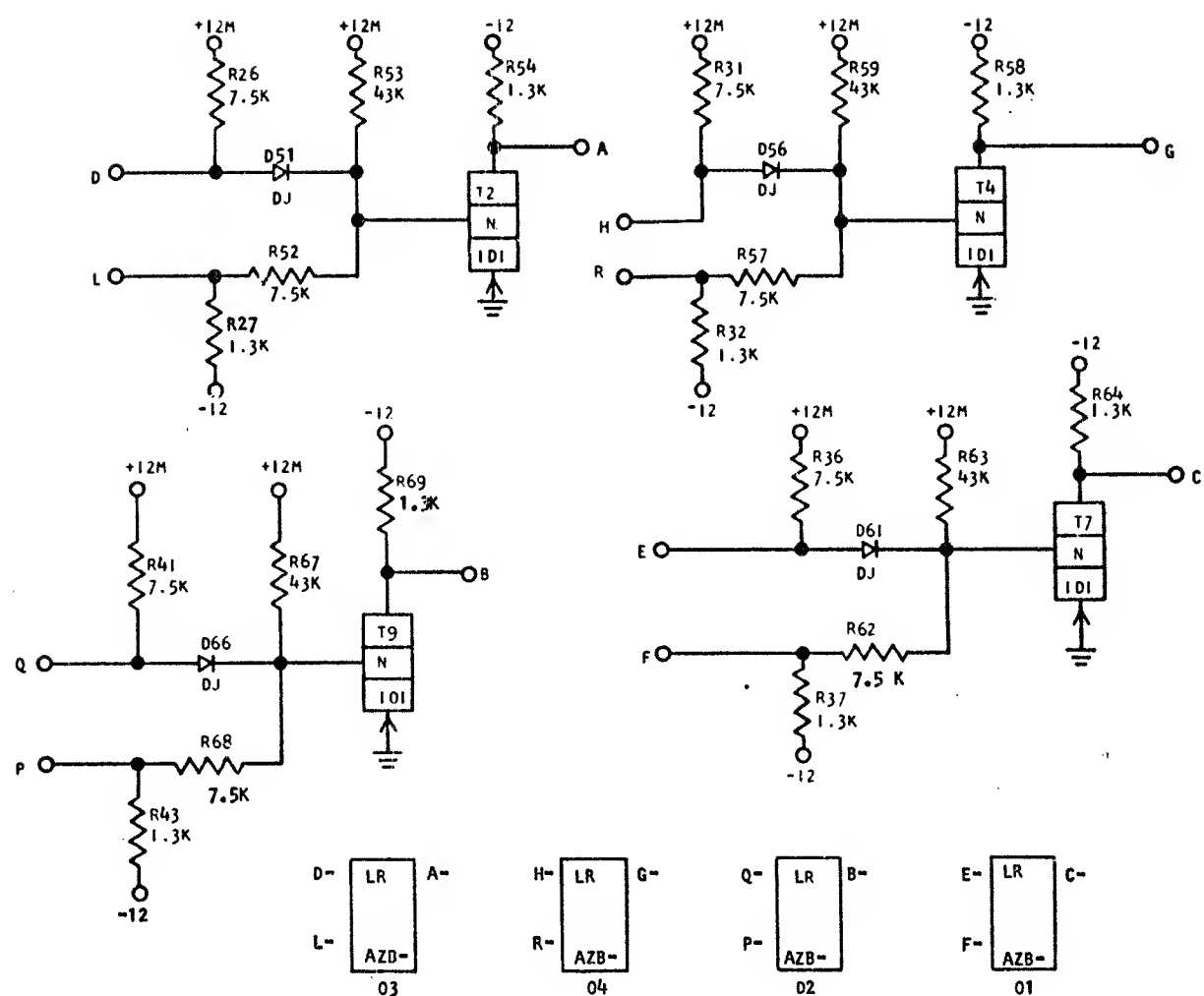
372321 REF.

BLOCKING CIRCUIT

AYZ



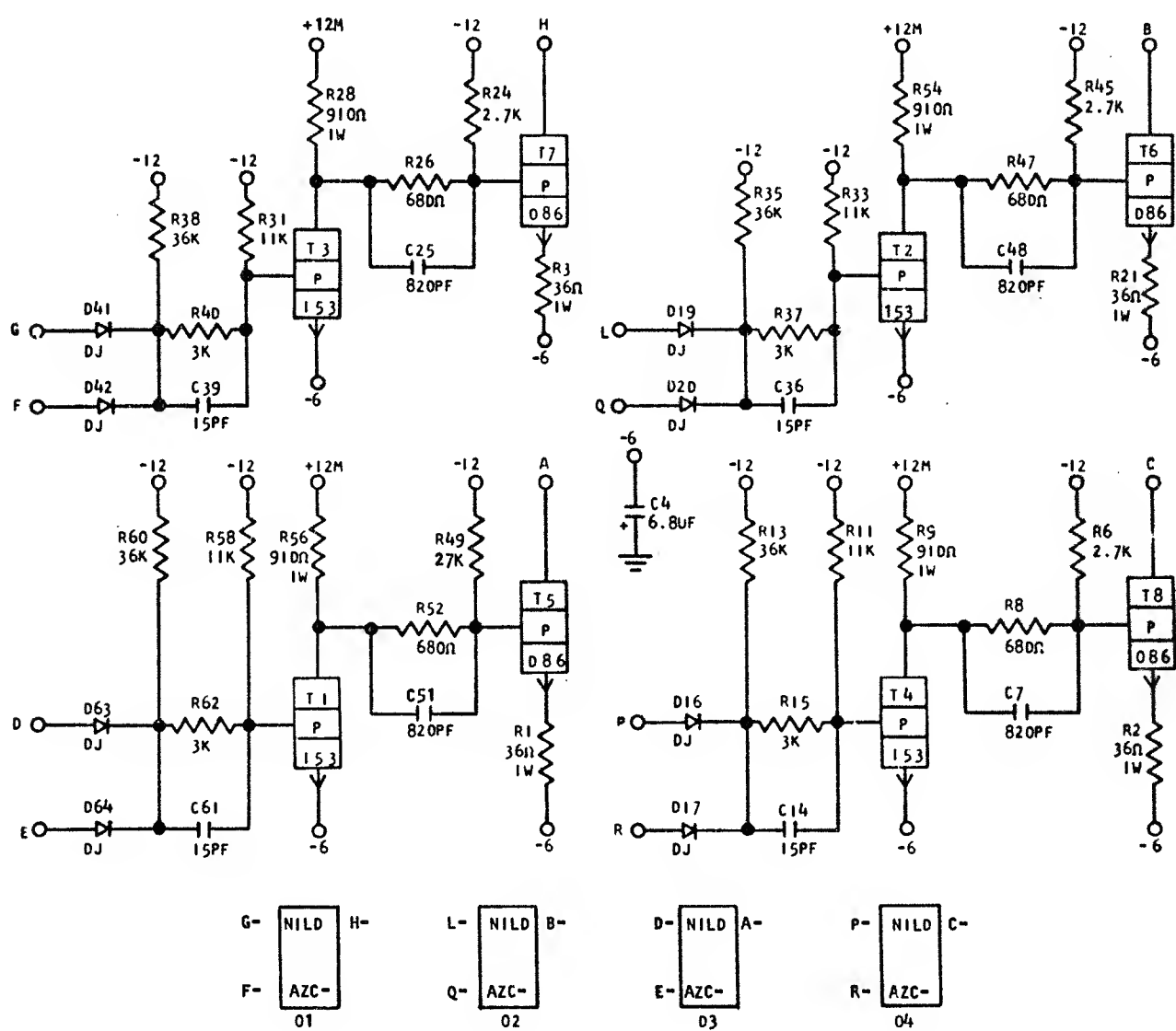
372320 REF.



372255 REF

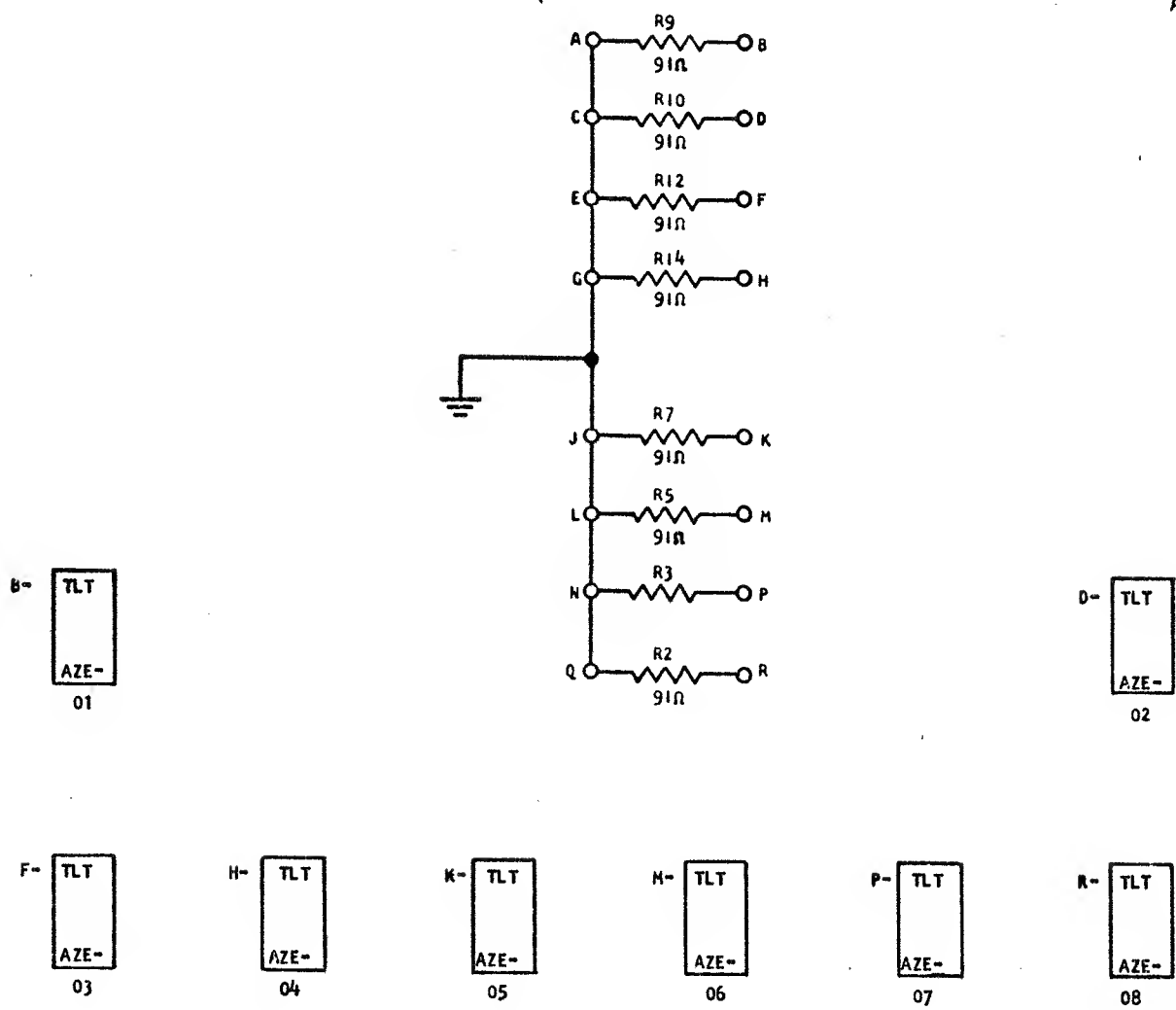
SDTDL NONINVERTING MULTIPLEX INTERFACE
(TWISTED PAIR) DRIVER

AZC



372256 REF

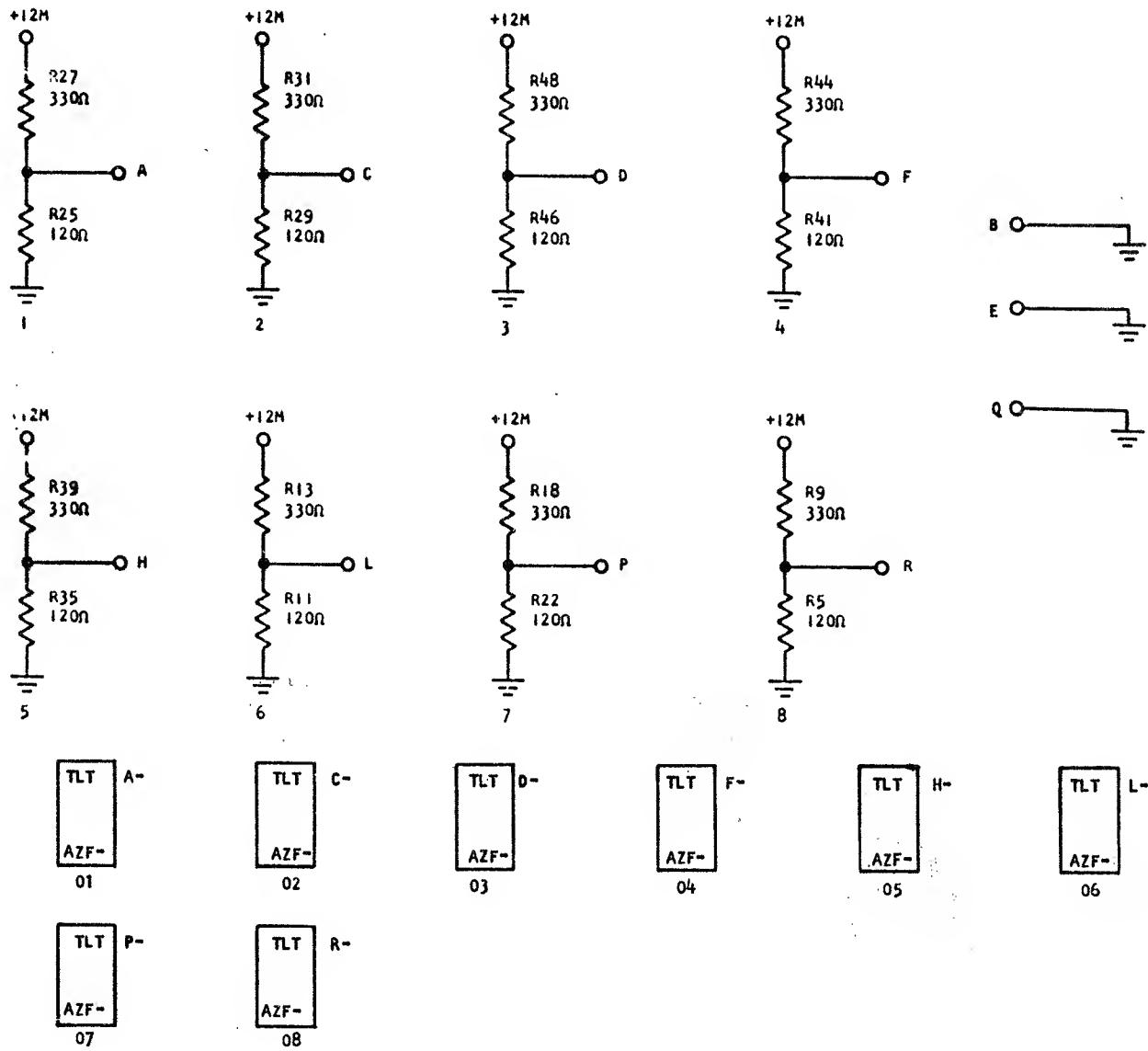
AZE



372258 REF

MULTIPLEX INTERFACE
TERMINATING NETWORK

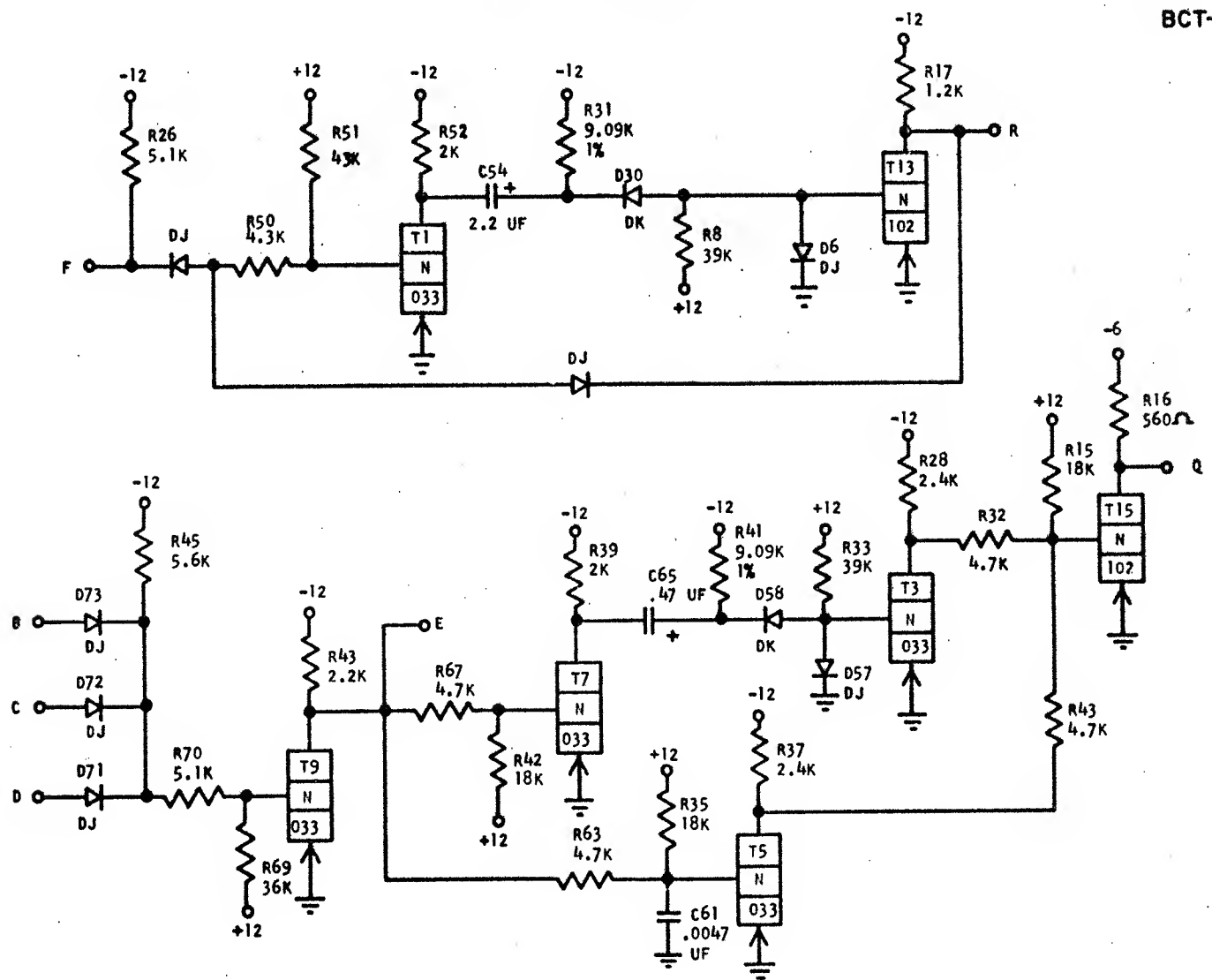
AZF



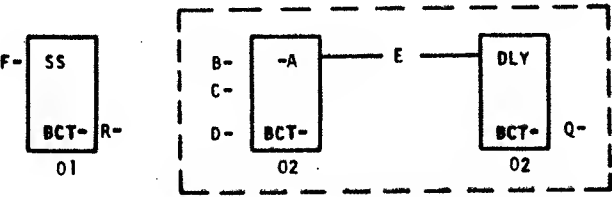
372259 REF

ACCESS TIMING

BCT-



372510 REF.

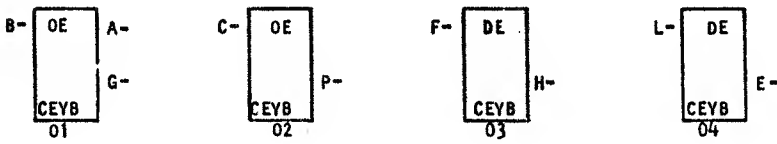
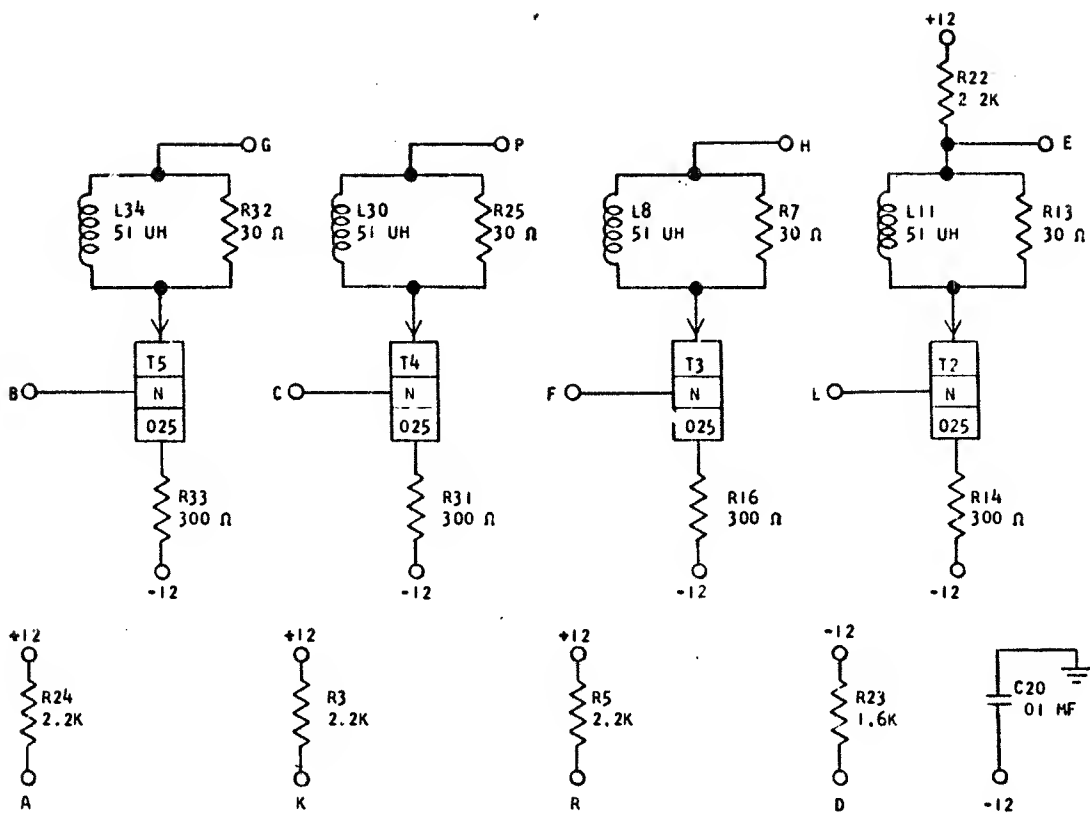


2157212

CTRL - EMITTER FOLLOWER PNP

1311

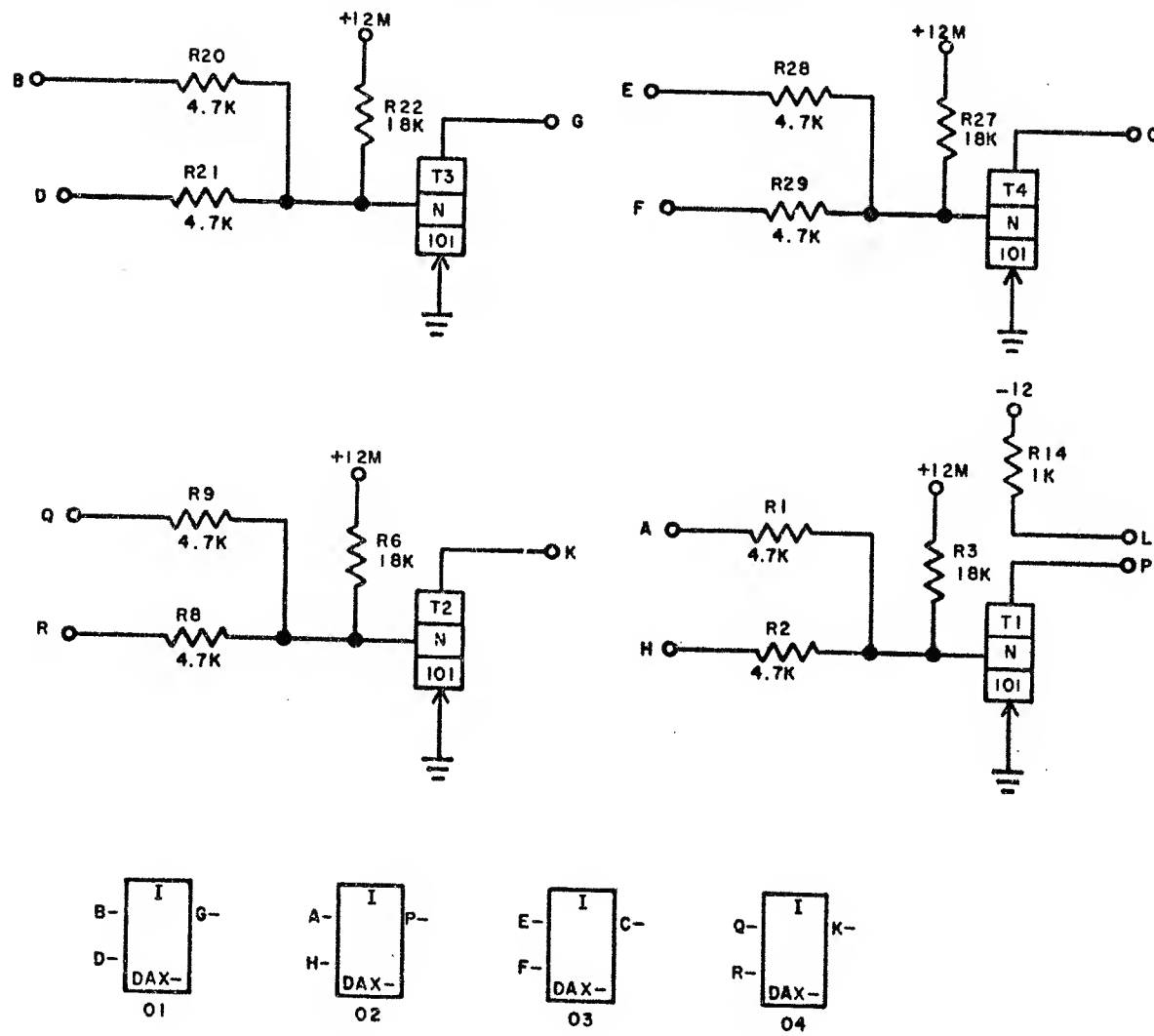
C2.90.12.0
CEYB



371032 REF

SDTRL - INVERTER, 2 WAY, UNLOADED COLLECTORS

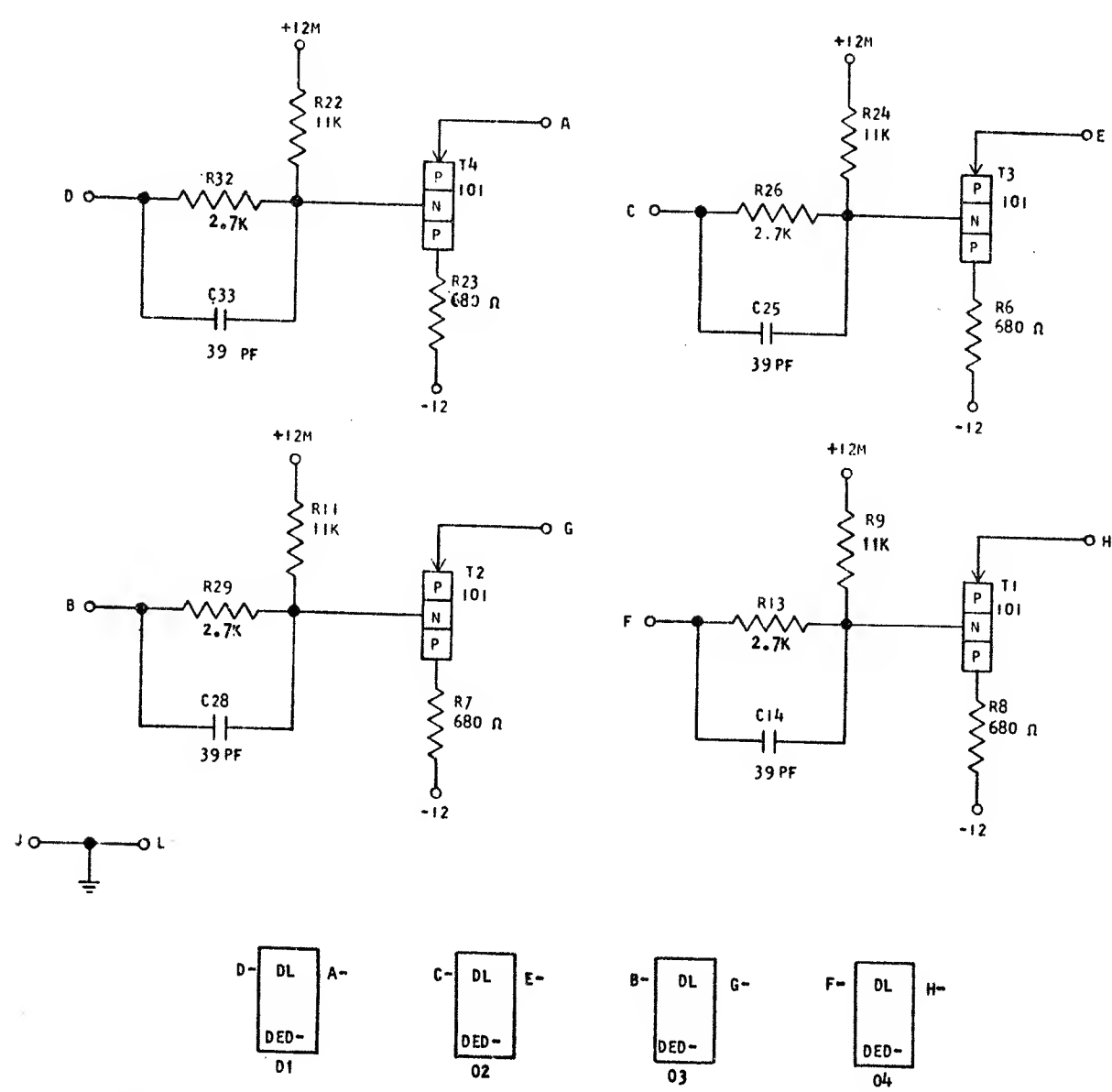
DAX -



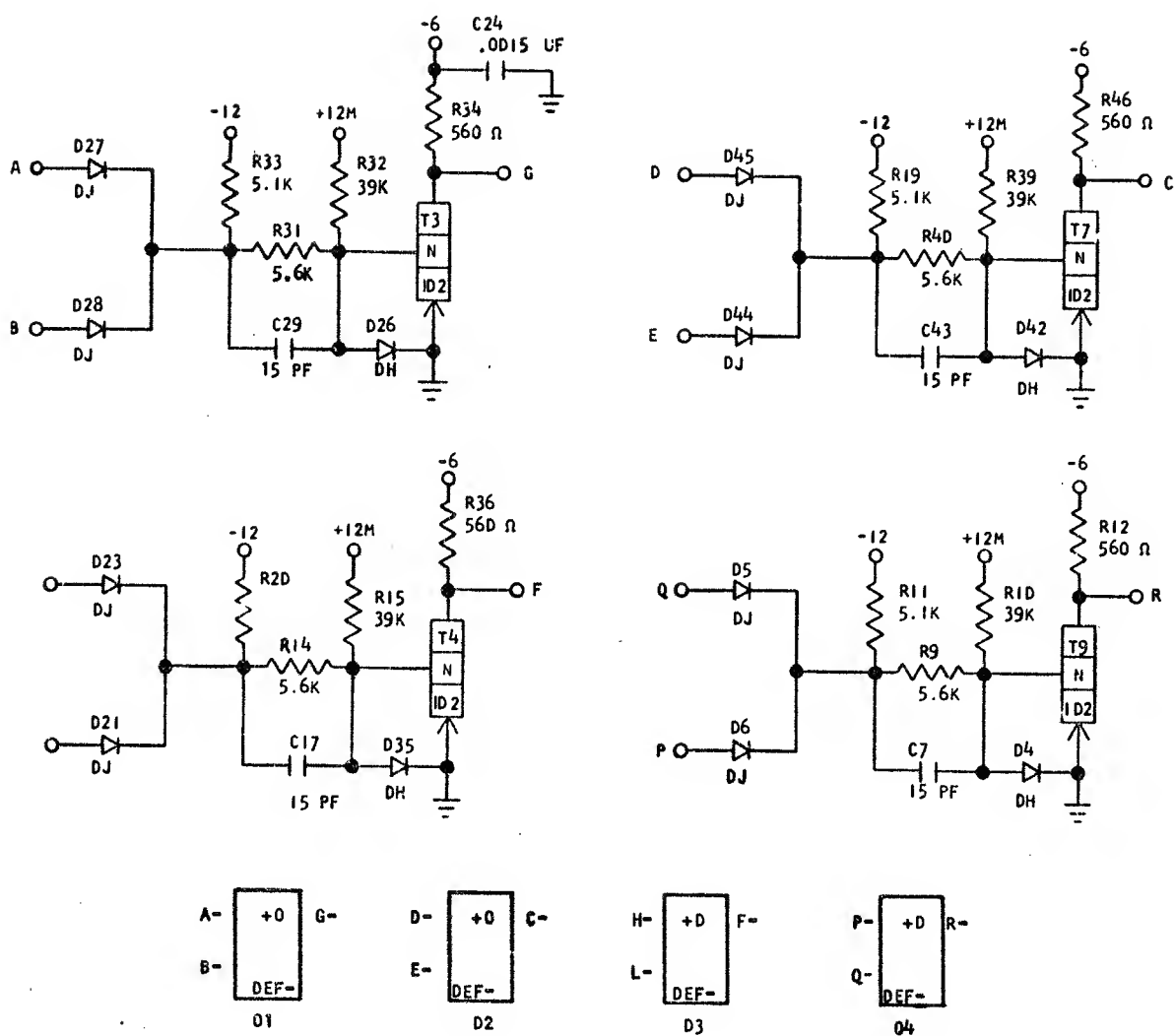
370084 REF

SDTRL - STANDARD CABLE DRIVER

DED

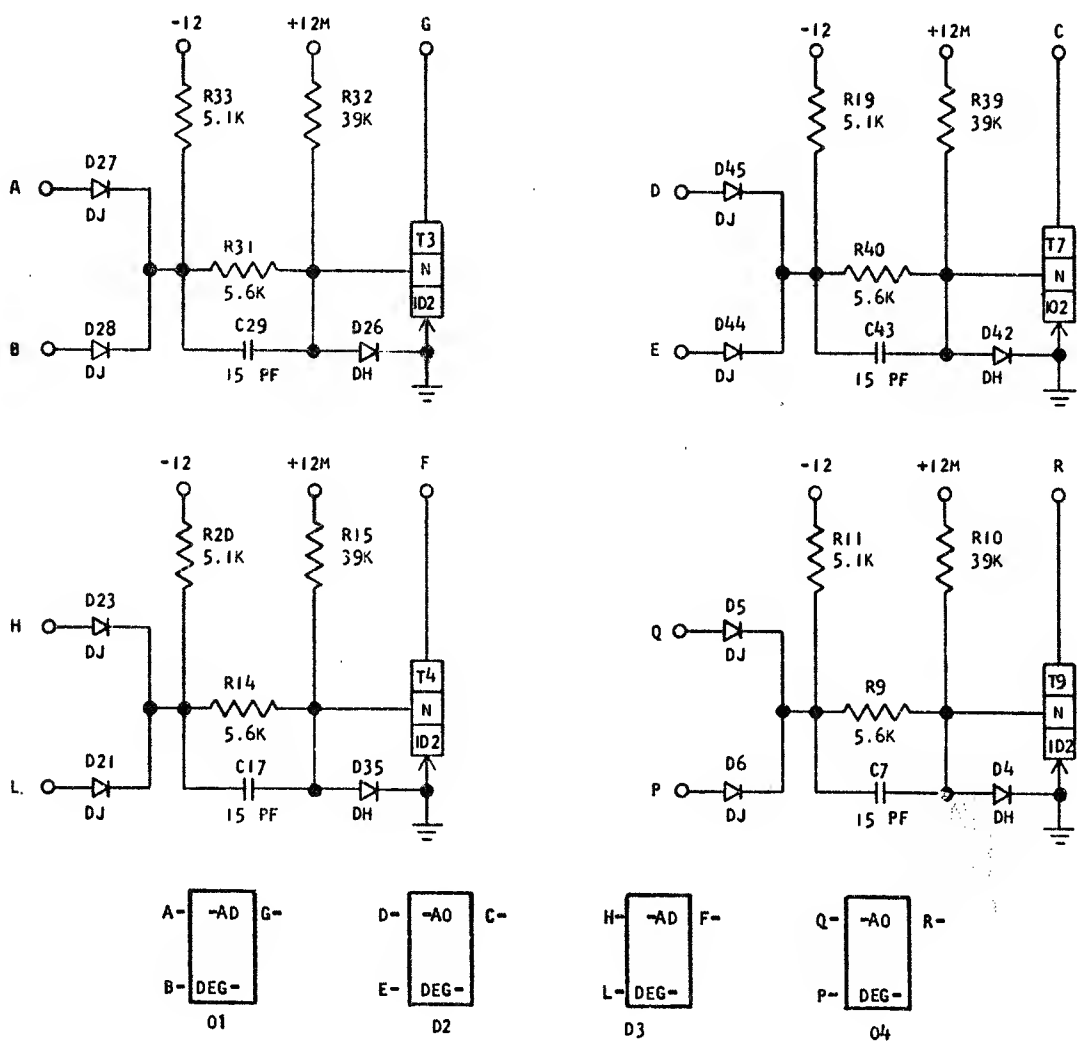


371987 REF

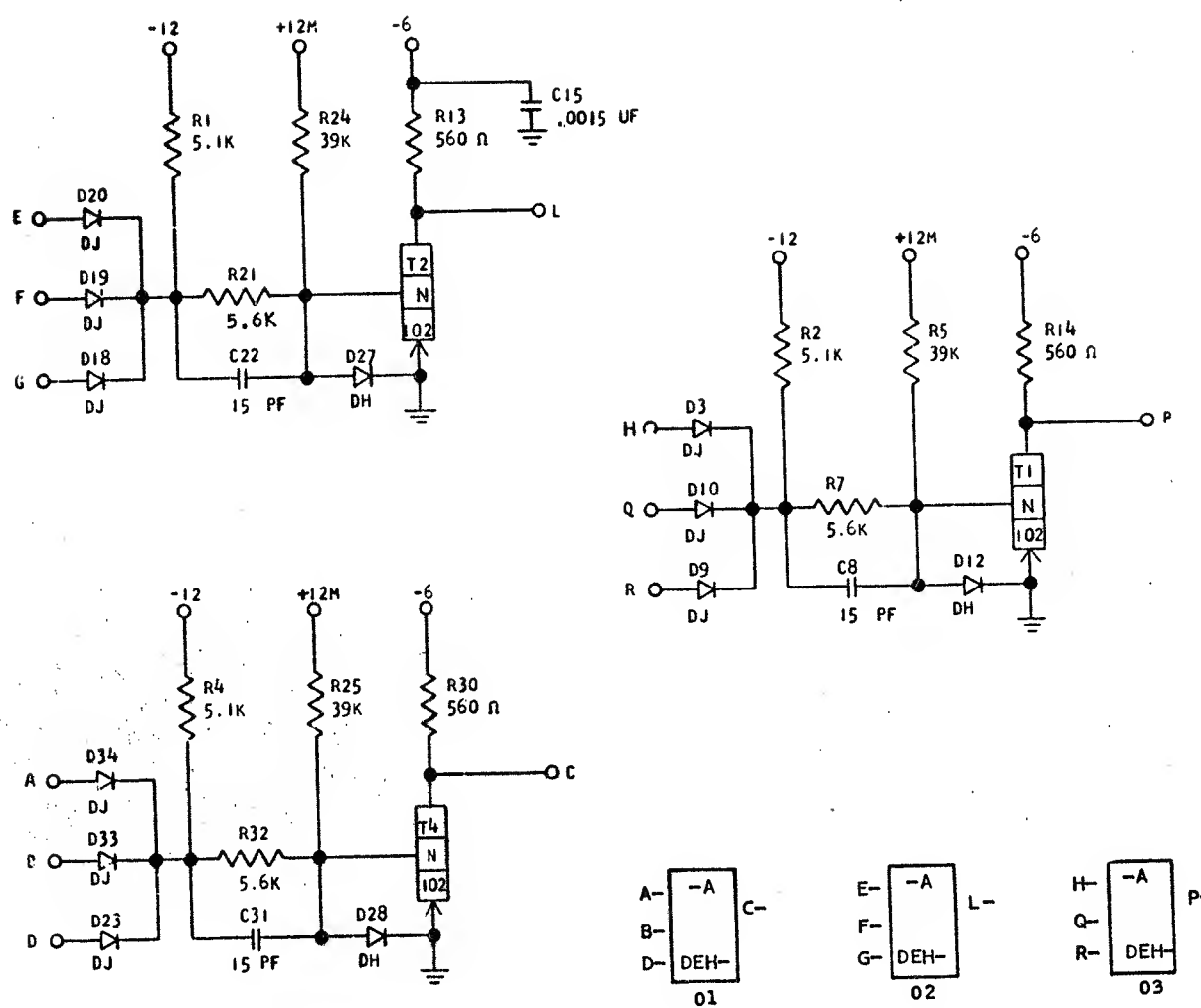


370216 REF

SDTDL FOUR 2-WAY N AND LOGIC BLOCKS WITHOUT LOADS

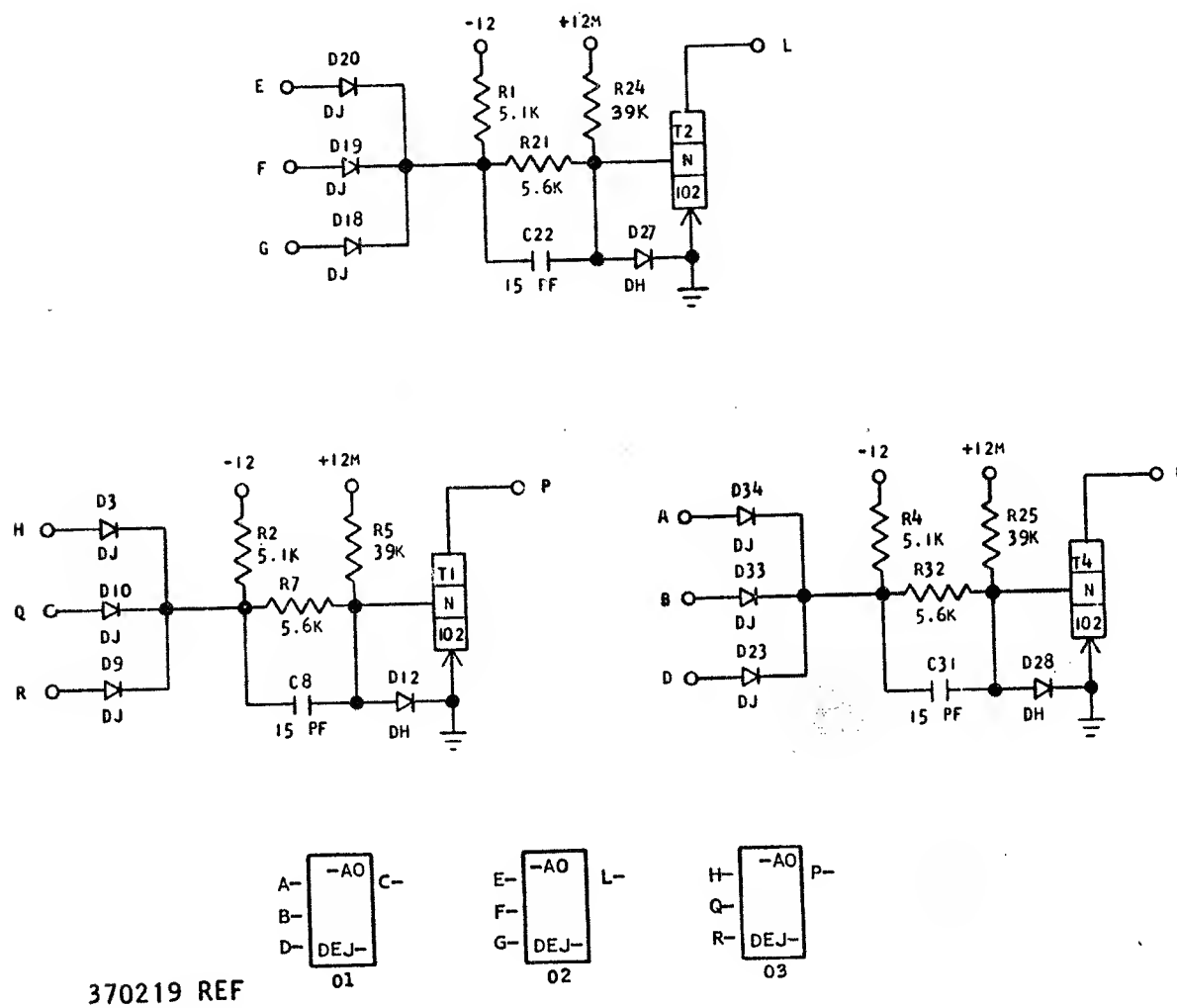


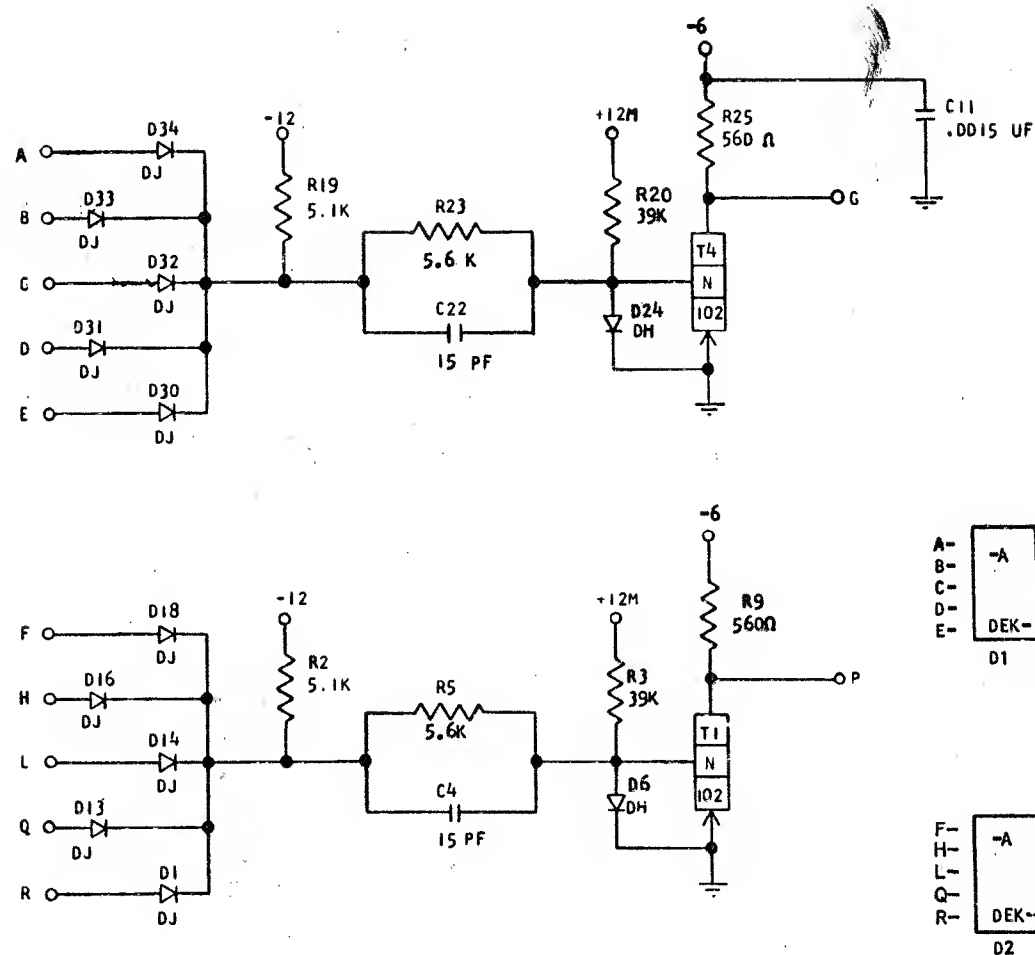
370217 REF



SDTDL THREE 3-WAY N AND LOGIC BLOCKS WITHOUT LOADS

DEJ

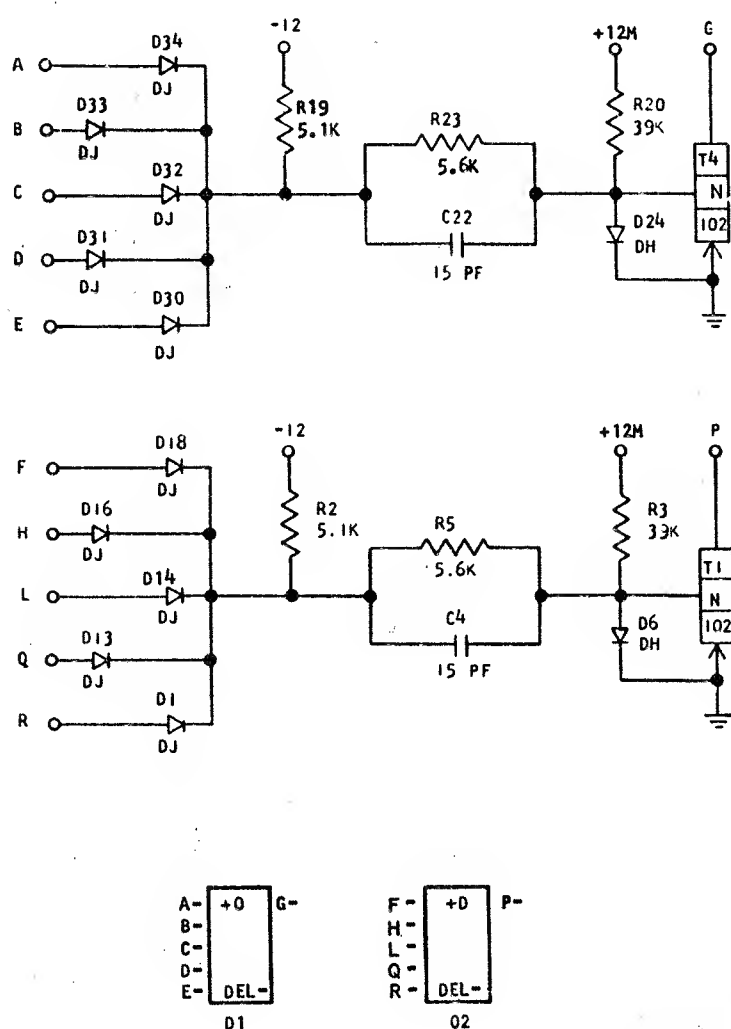




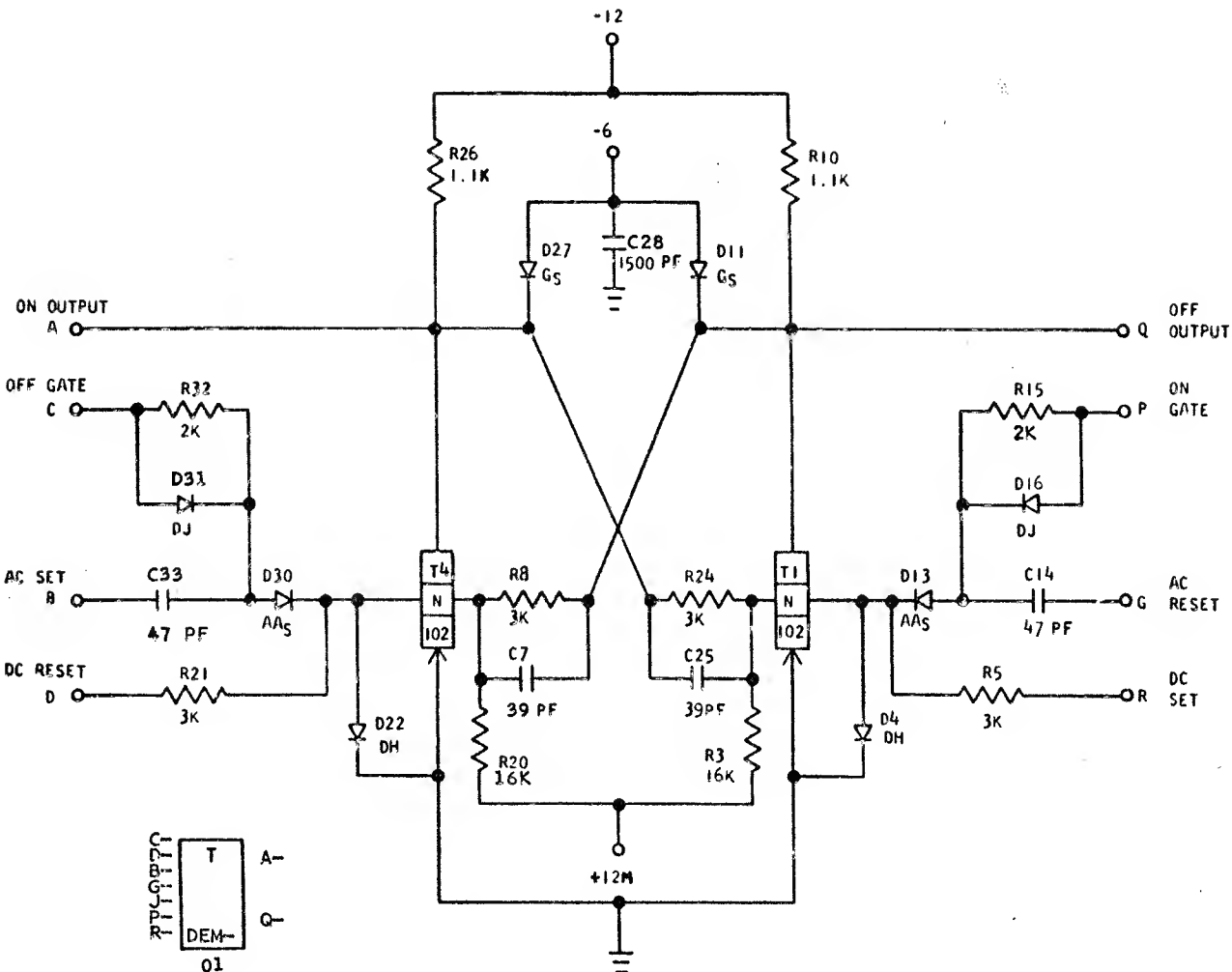
370220 REF

SDTDL TWO 5-WAY N AND LOGIC BLOCKS WITHOUT LOADS

DEL



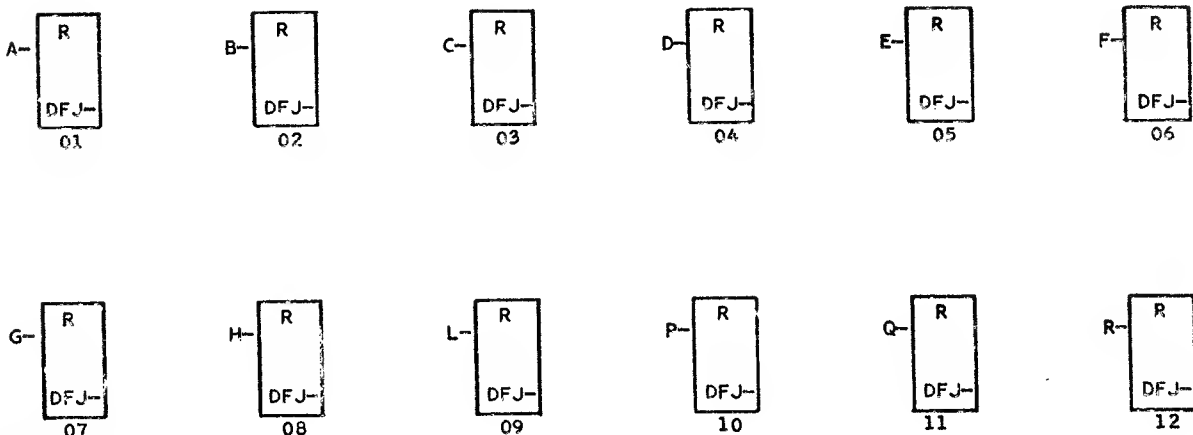
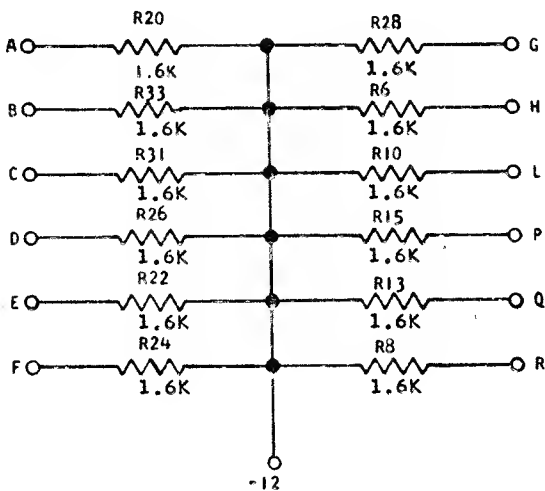
370221 REF



370222 REF

TDL & TRL LOAD CARD

DFJ



370232 REF

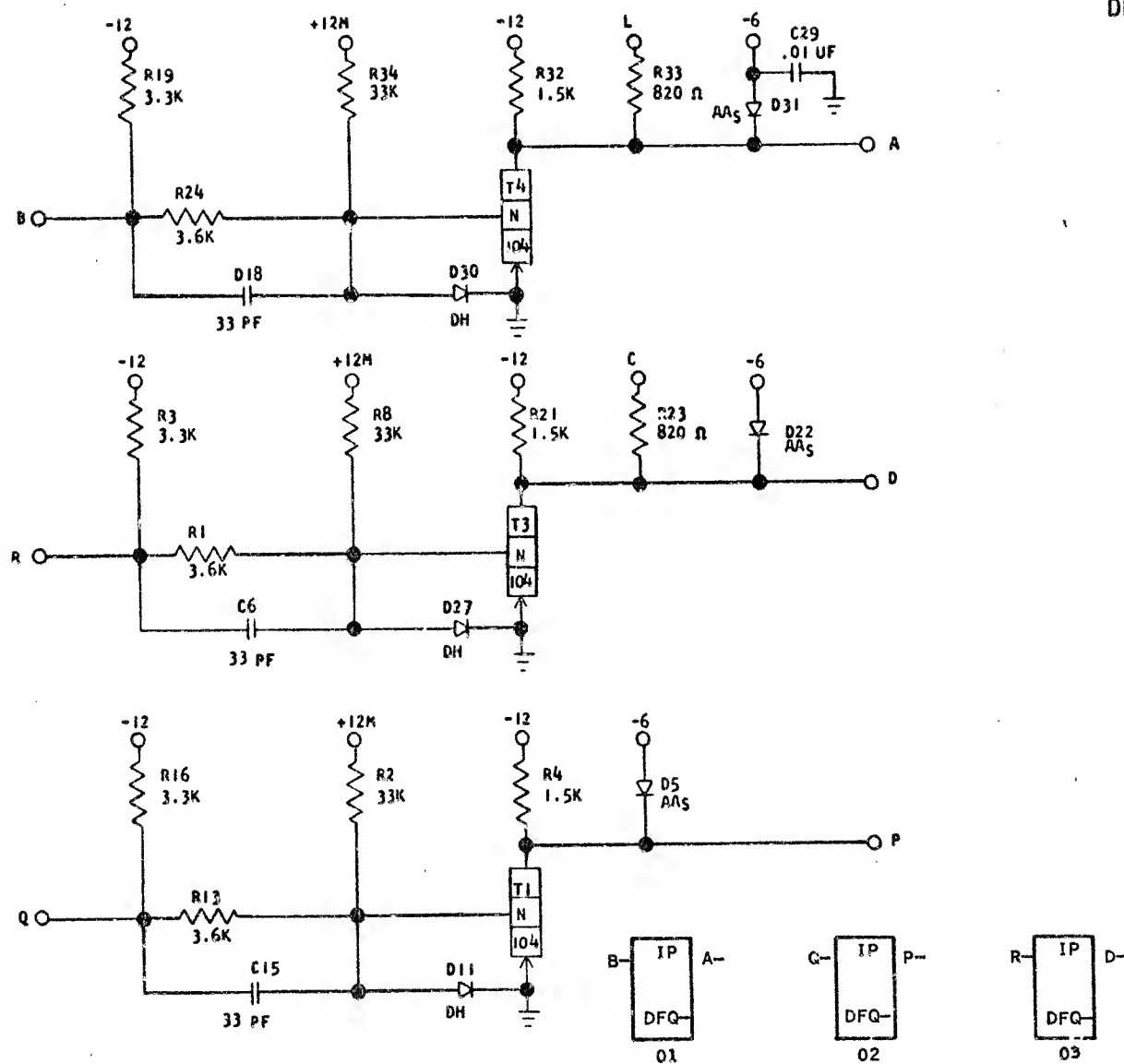
2157217

SDTDL INVERTING POWER DRIVER

1311

C2.90.17.0

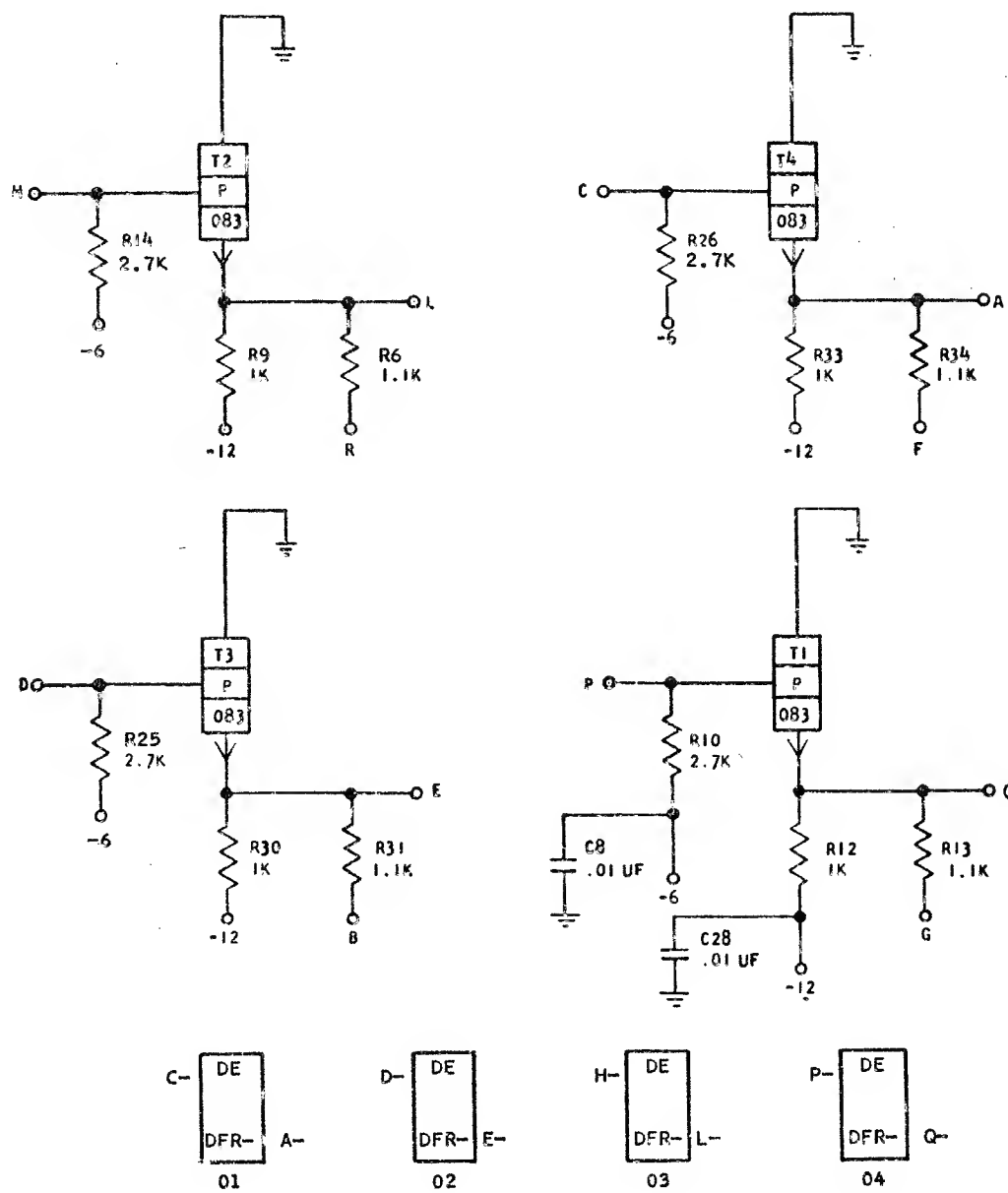
DFQ



370225 REF

SDTDL NON-INVERTING POWER DRIVER

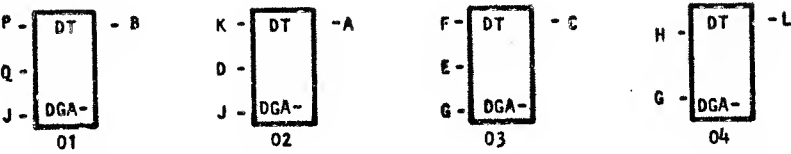
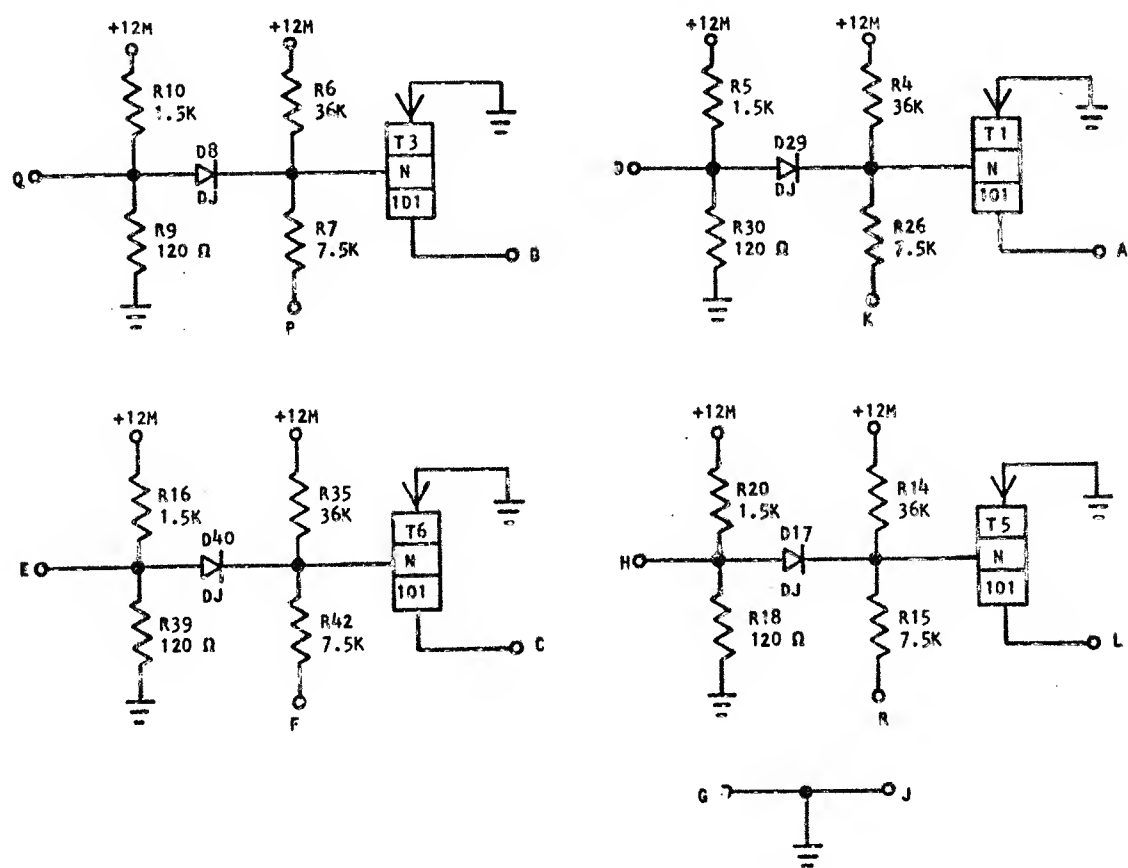
DFR



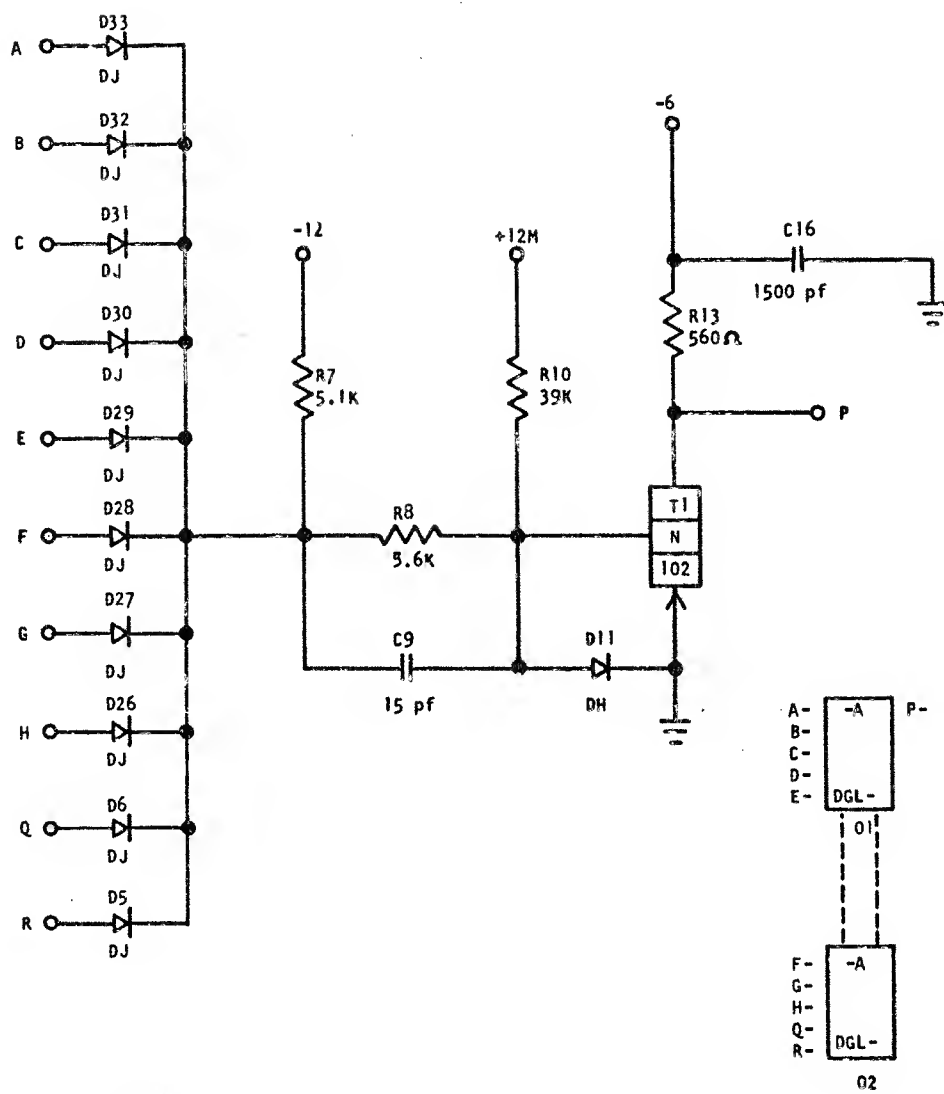
370226 REF

DGA-

SDTRL - SIMPLEX INTERFACE TERMINATOR
GATED WITHOUT LOADS

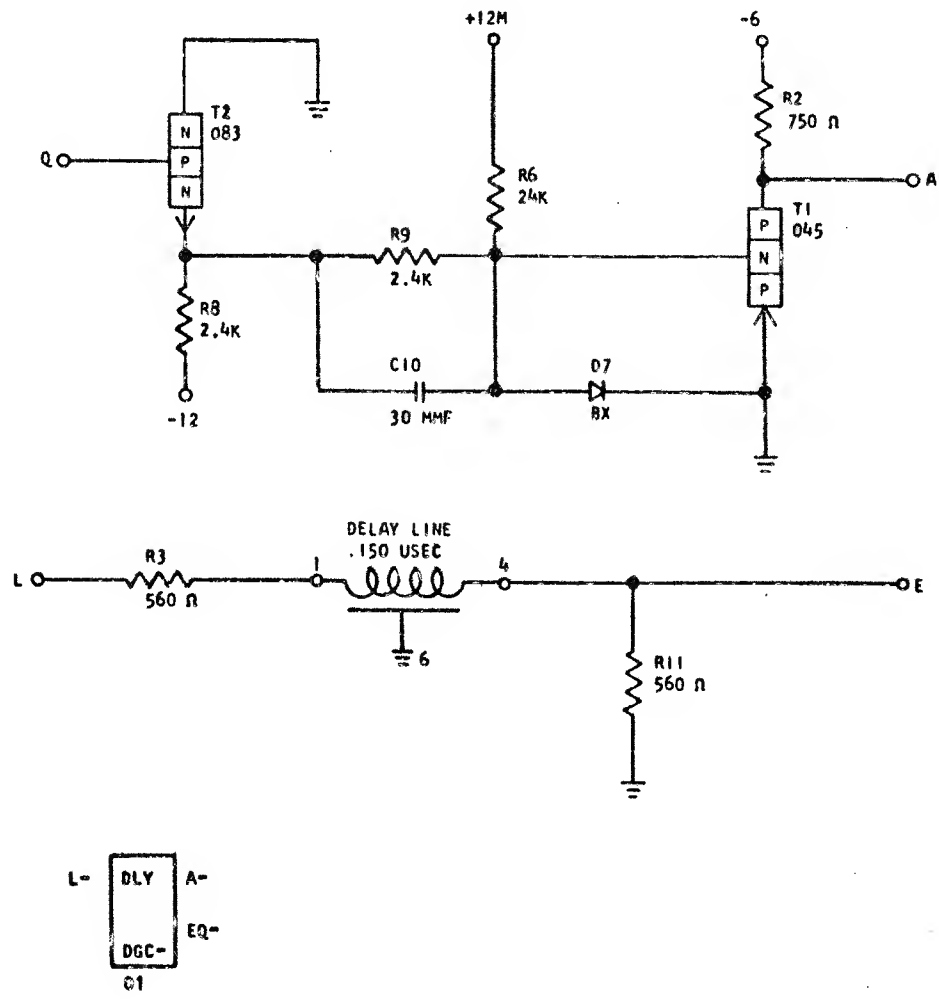


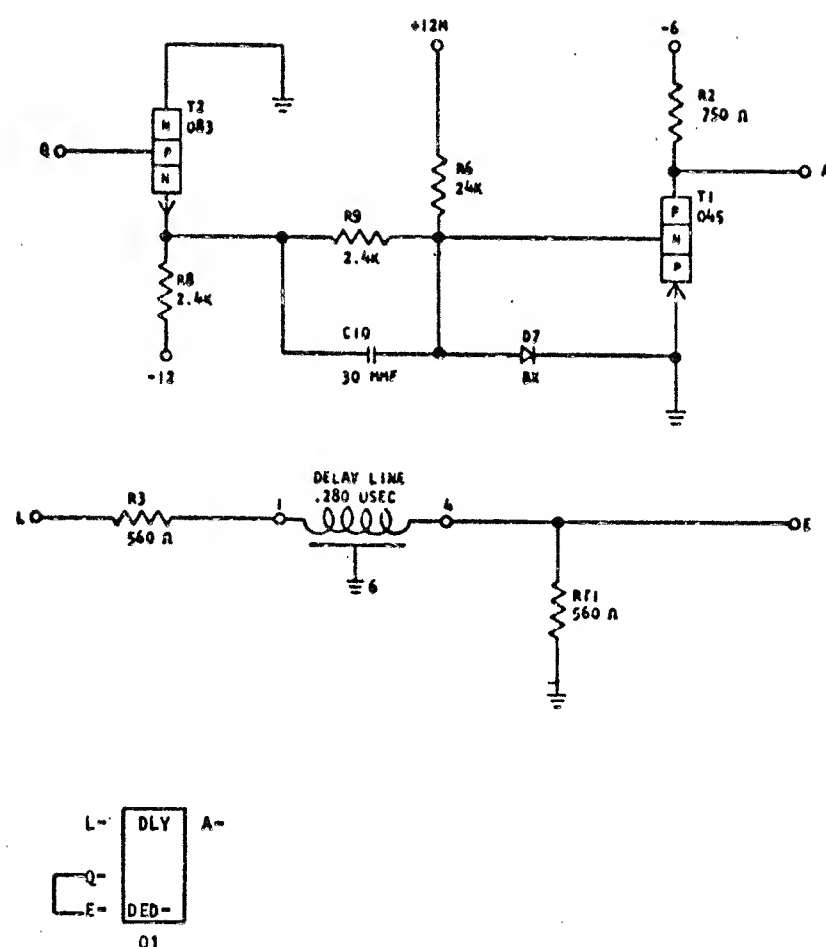
370242 REF



SDTDL MEMORY .150 USEC DELAY LINE

DGC

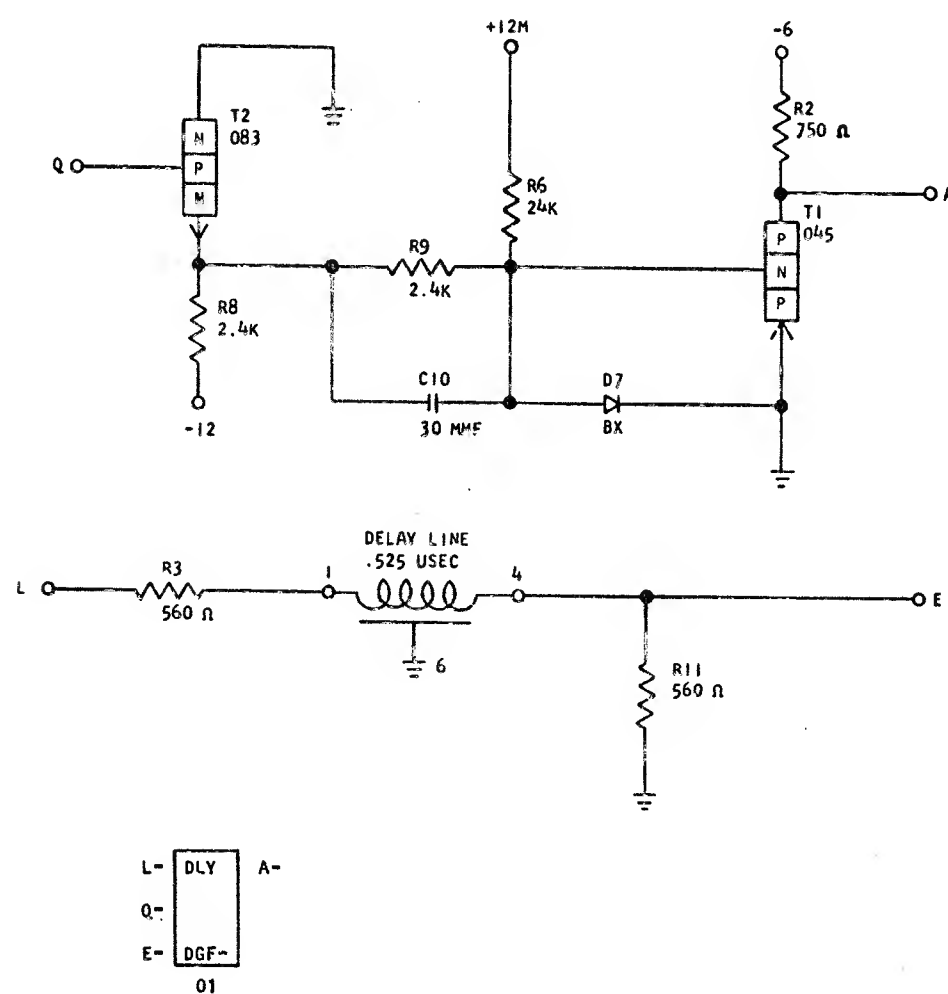




370245 REF

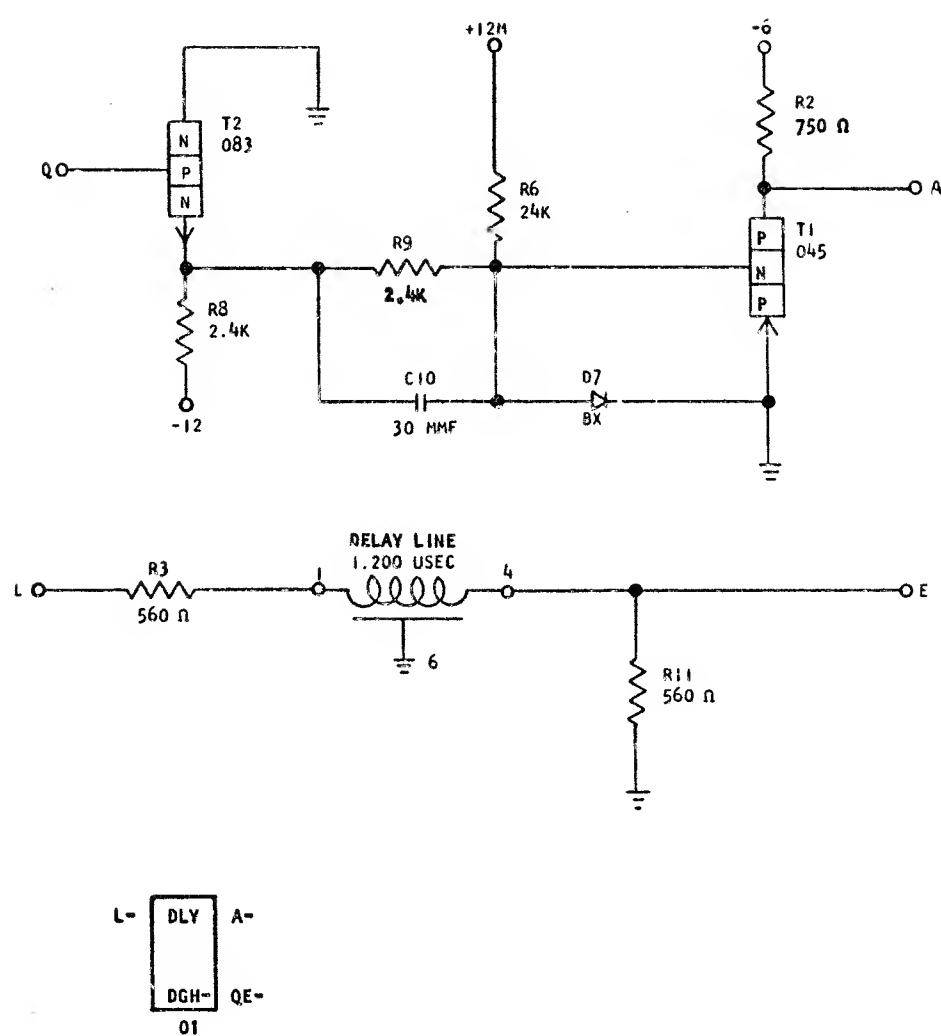
SDTDL MEMORY .525 USEC DELAY LINE

DGF



370247 REF

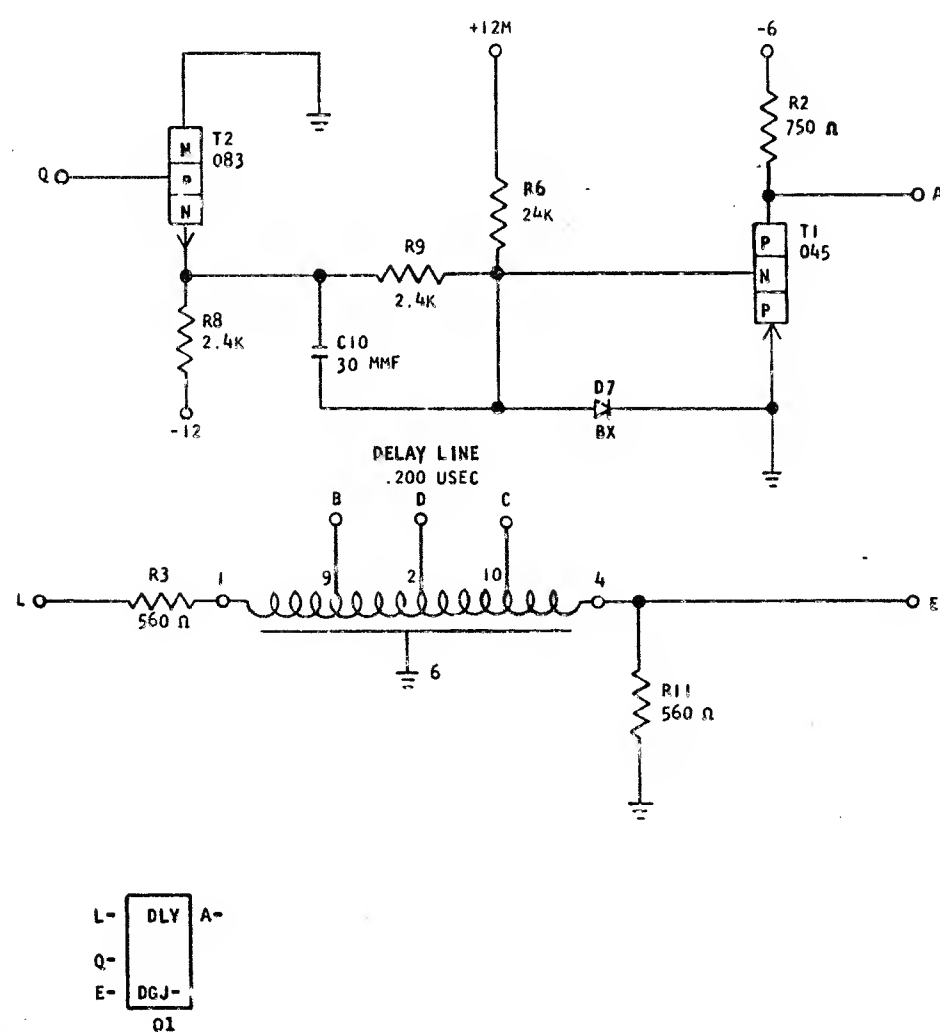
DGH



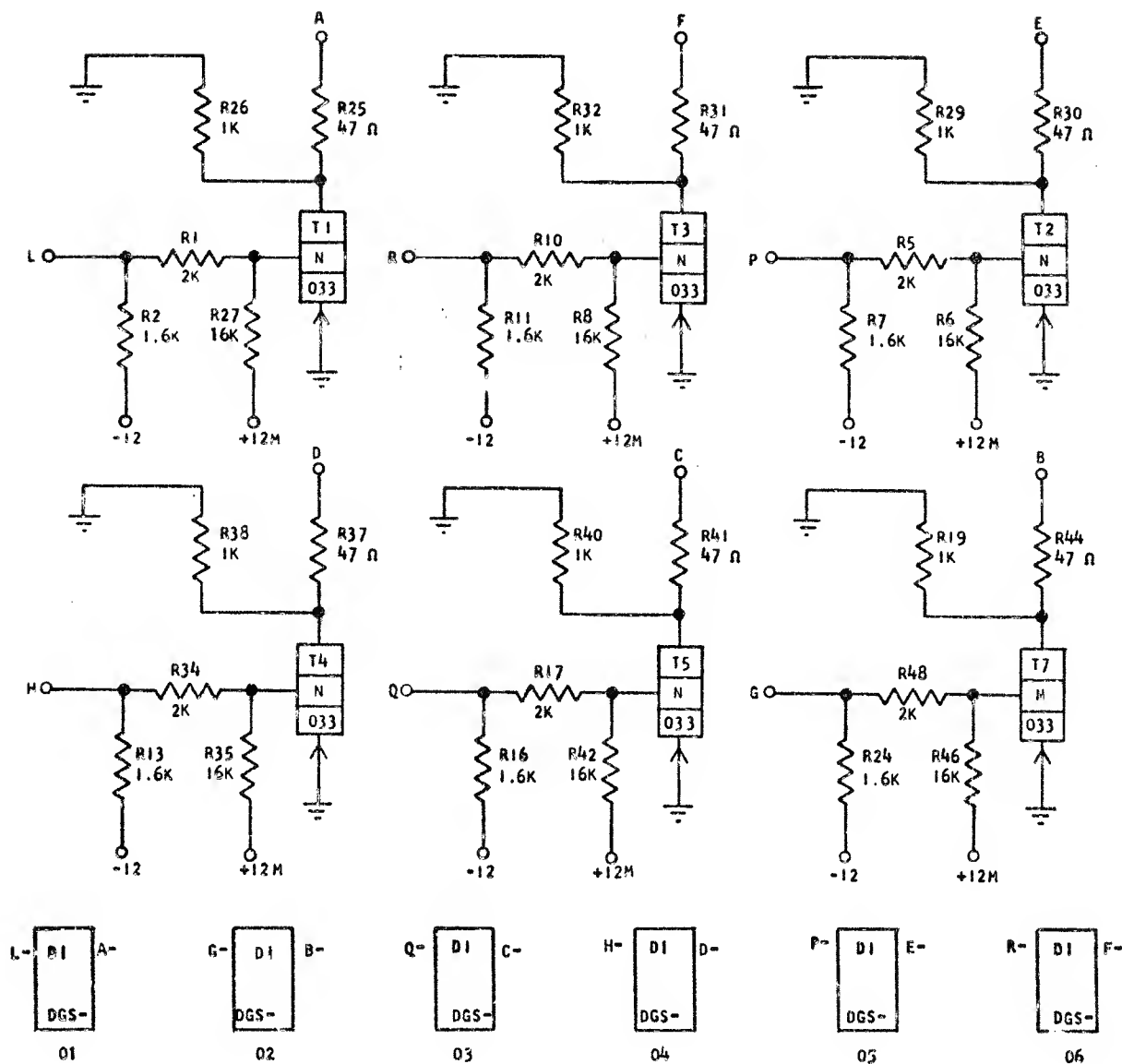
370249 REF

SDTDL MEMORY .200 USEC DELAY LINE

DGJ



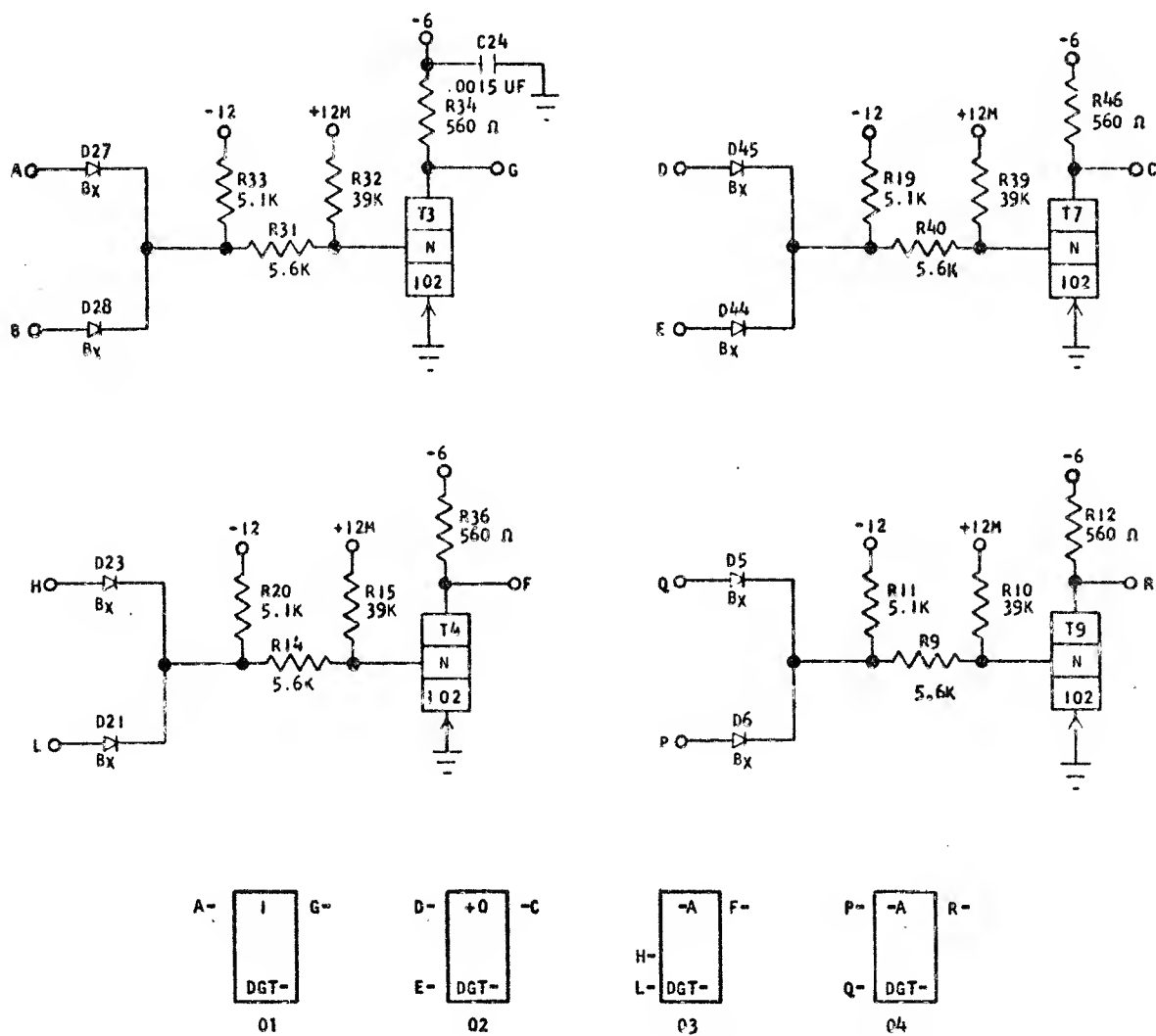
370250 REF



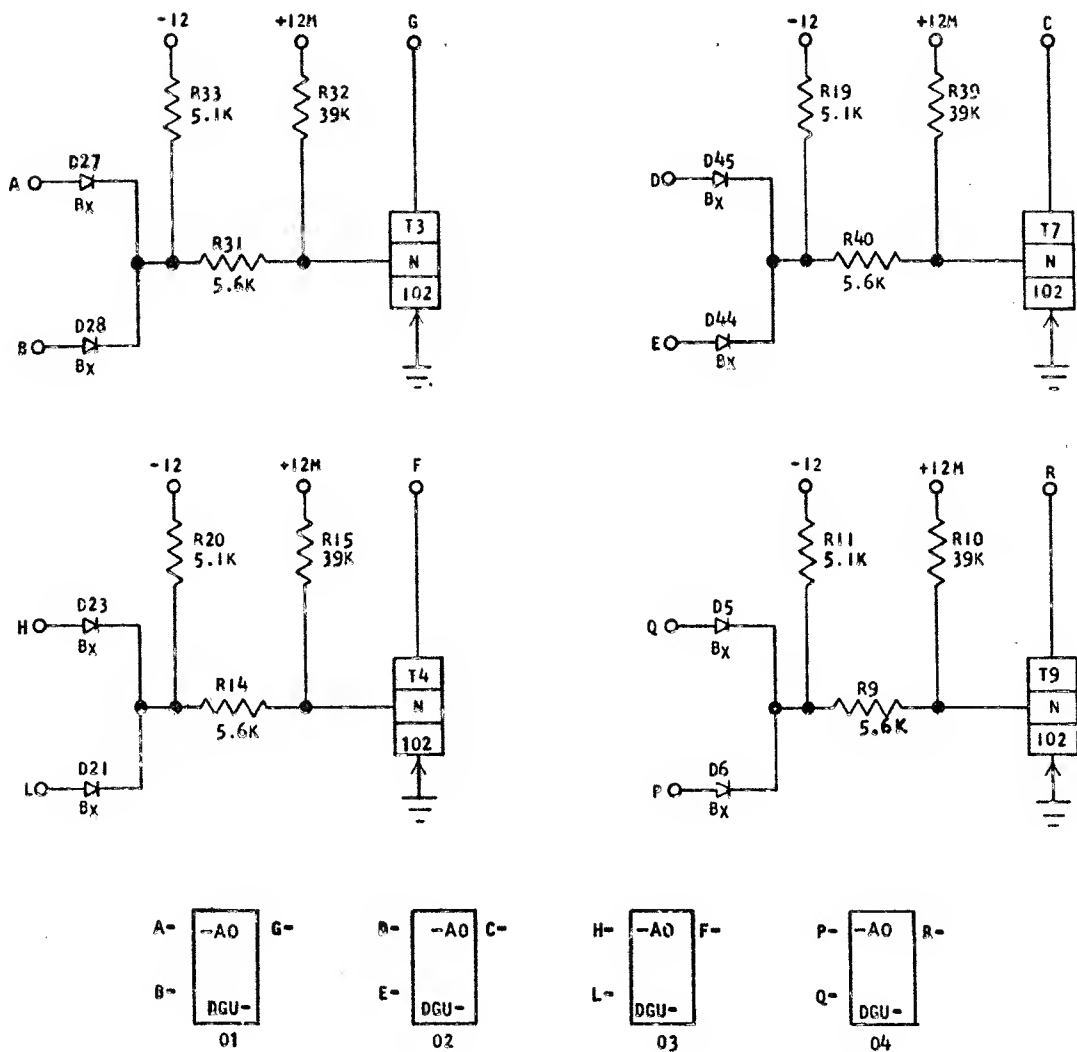
370347 REF

SDTDL-2 WAY LOGIC BLOCK LOW SPEED WITH LOADS

DGT

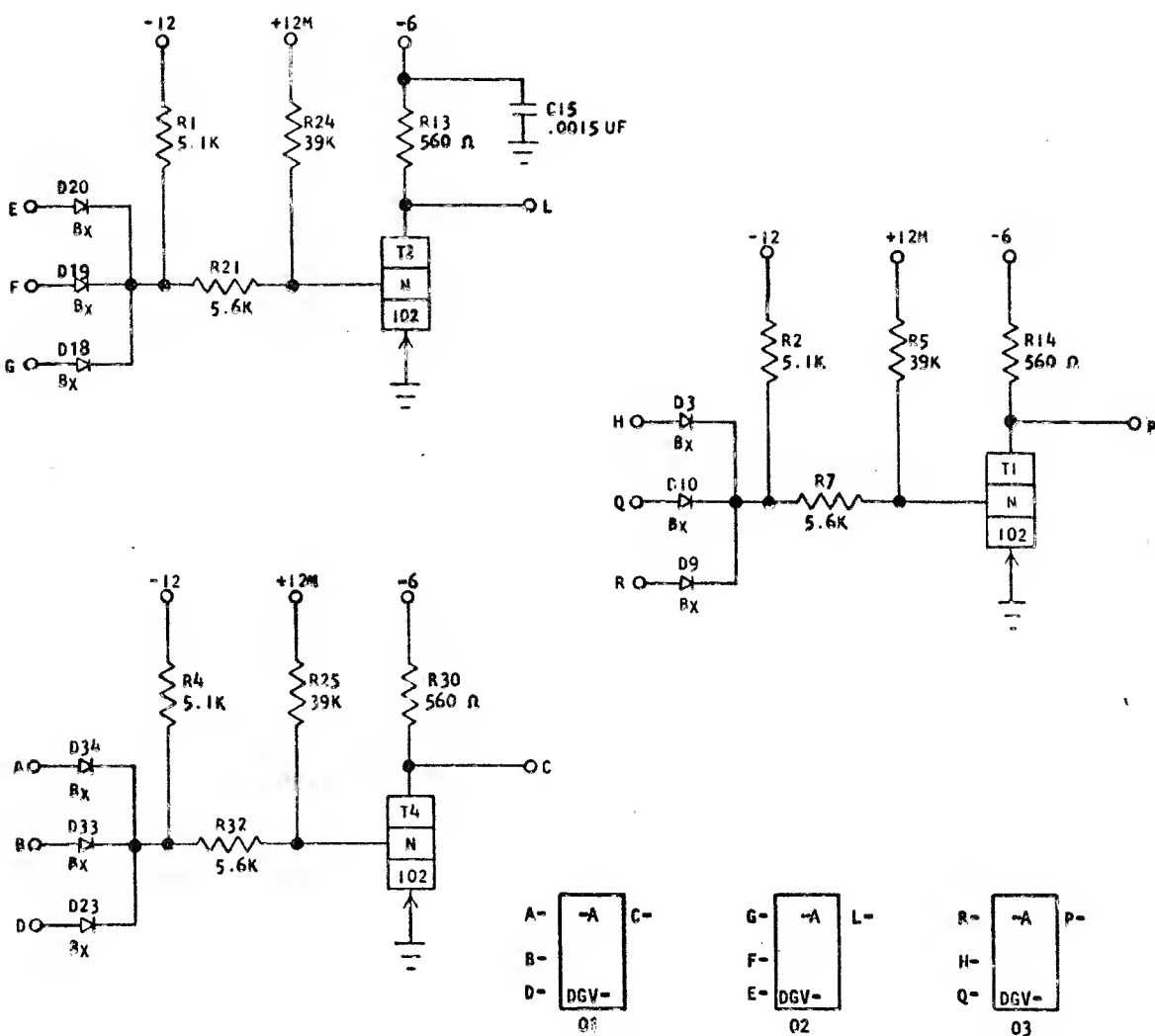


370380 REF

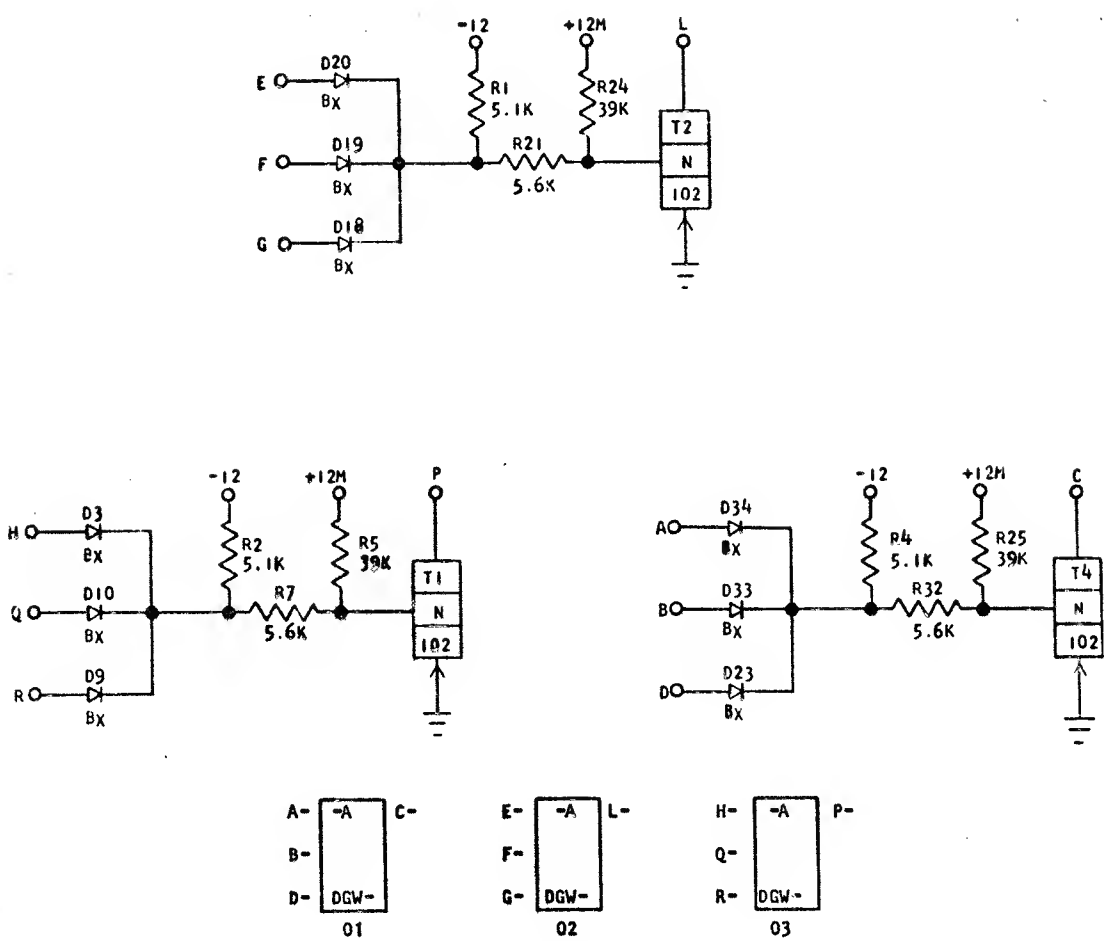


370379 REF

SDTDL - 3-WAY LOGIC BLOCK LOW SPEED WITH LOADS DGV



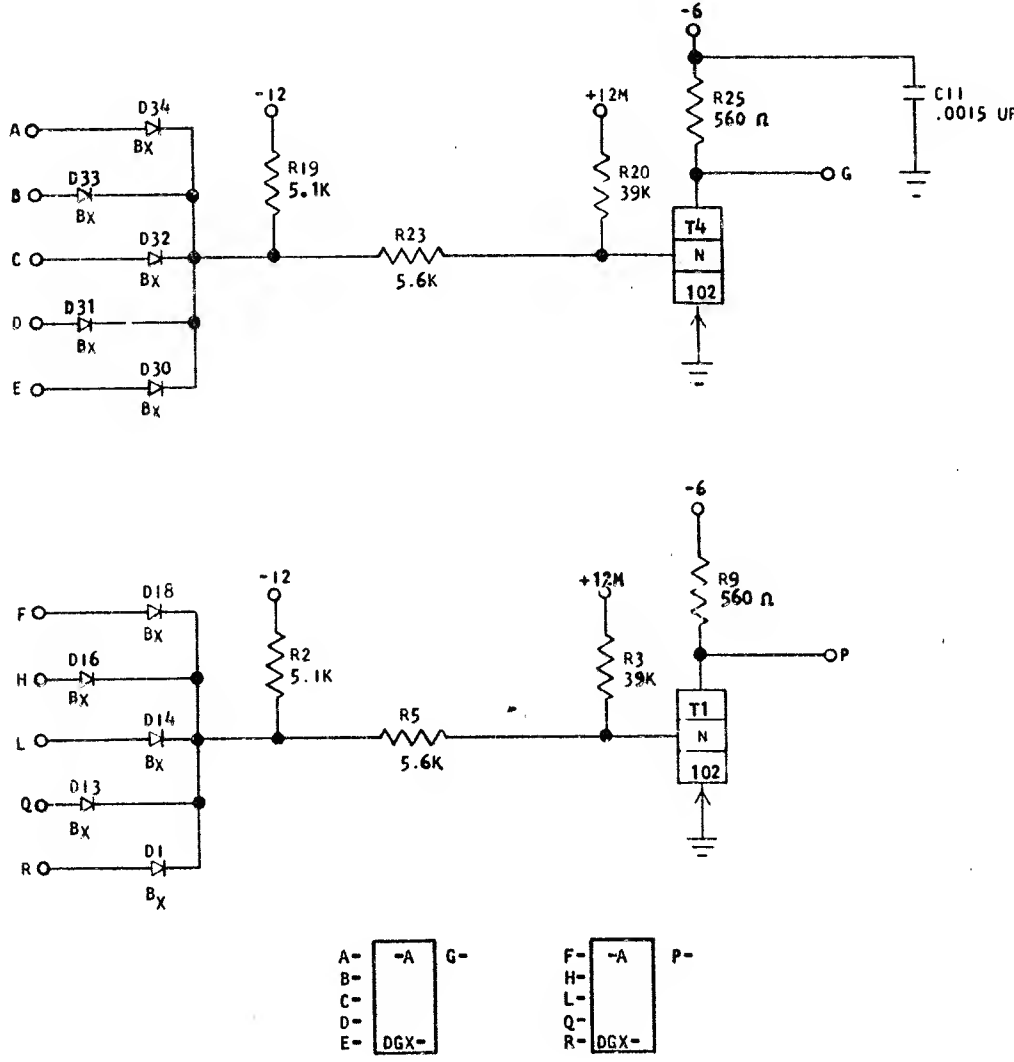
370378 REF



370377 REF

SDTDL-5-WAY LOGIC BLOCK LOW SPEED WITH LOADS

DGX



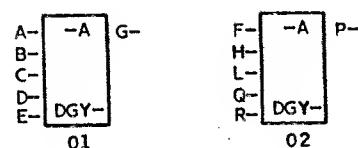
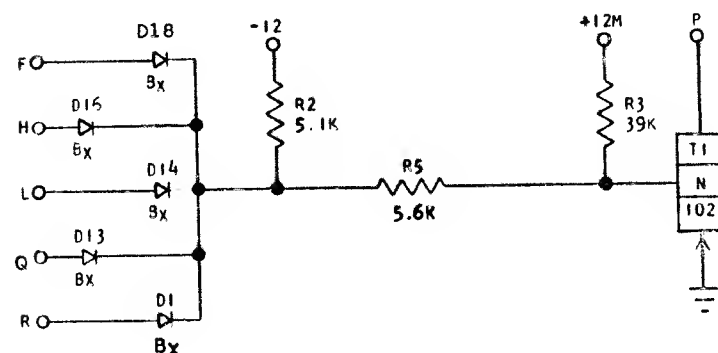
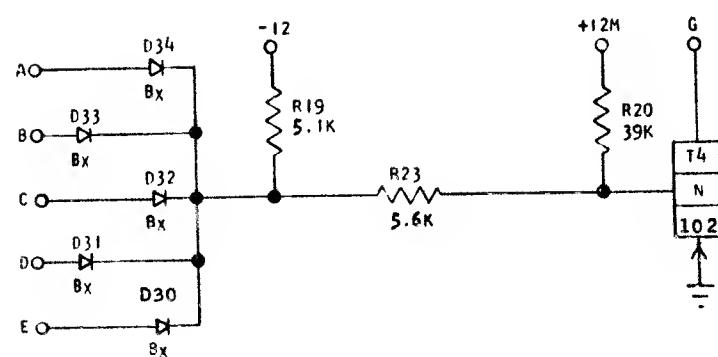
370376 REF

2157223

SDTDL 5 WAY LOGIC BLOCK LOW SPEED WITHOUT LOAD

1311 C2.90.23.0

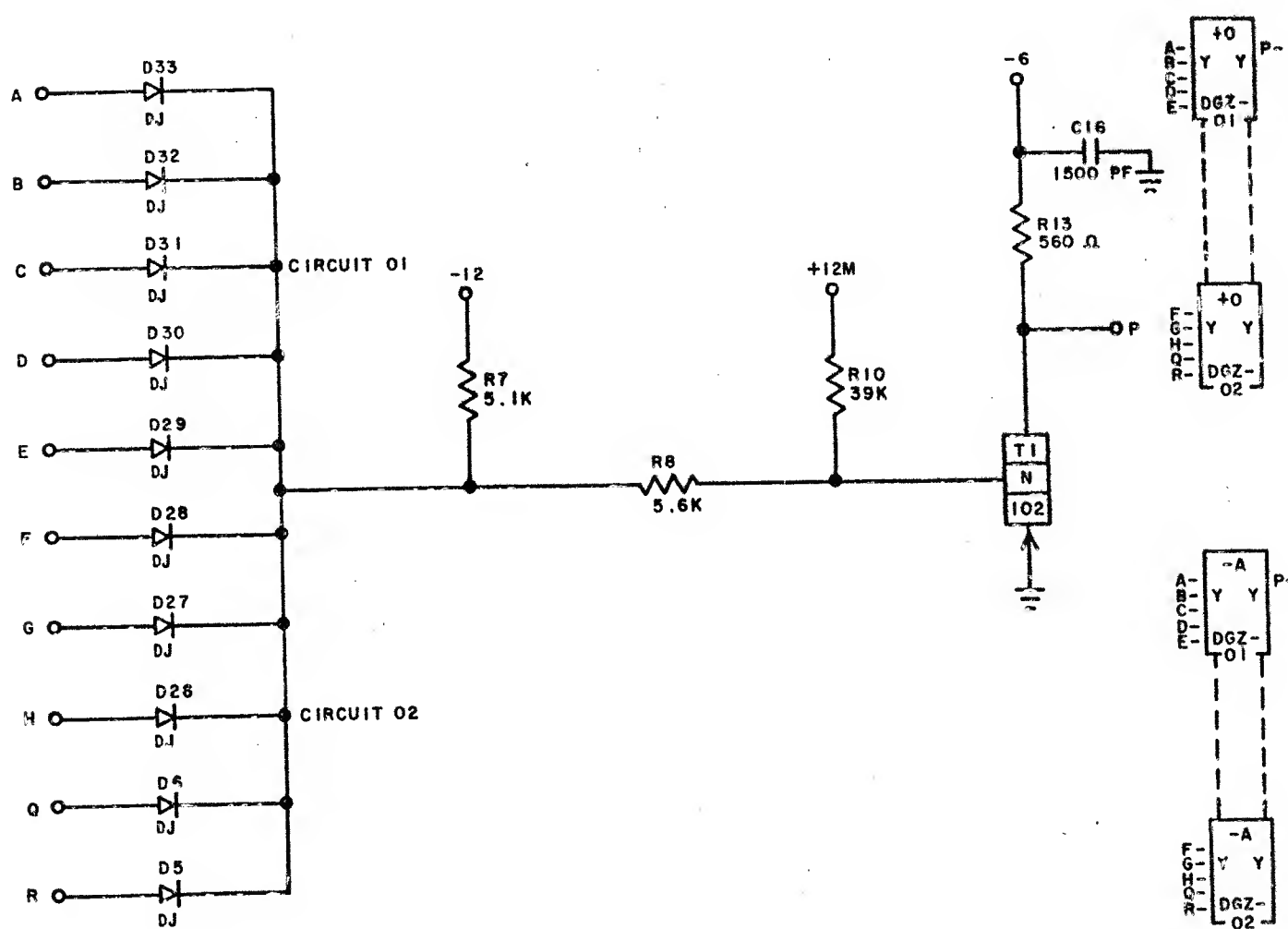
DGY



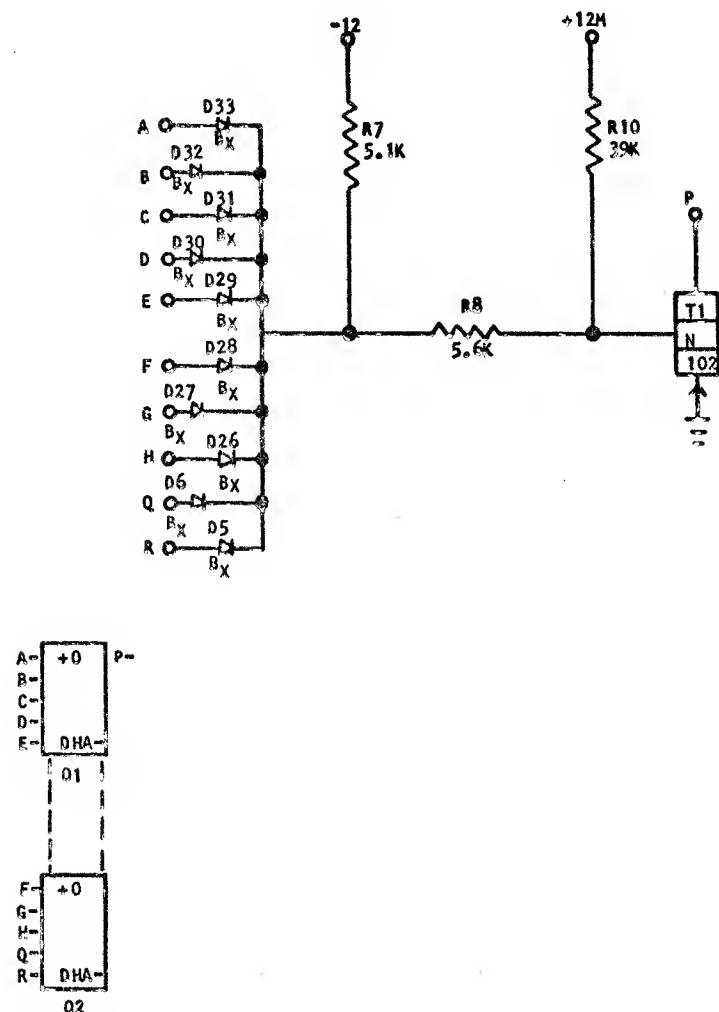
370375 REF

SDTDL 10-WAY LOGIC BLOCK LOW SPEED WITH LOAD

DGZ-

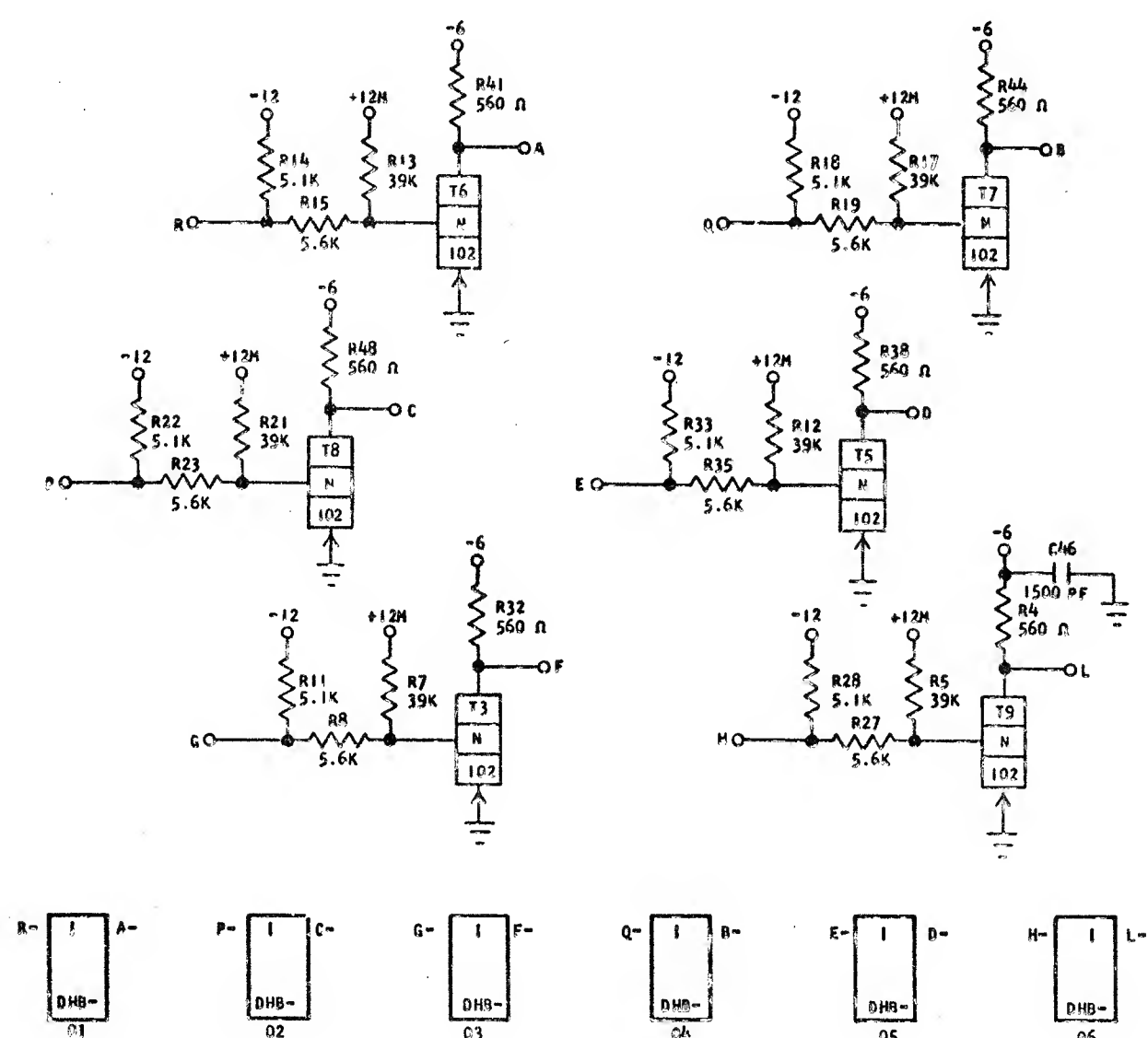


370373 REF



370374 REF

SDTDL INVERTER LOW SPEED WITH LOAD DHB



370348 REF

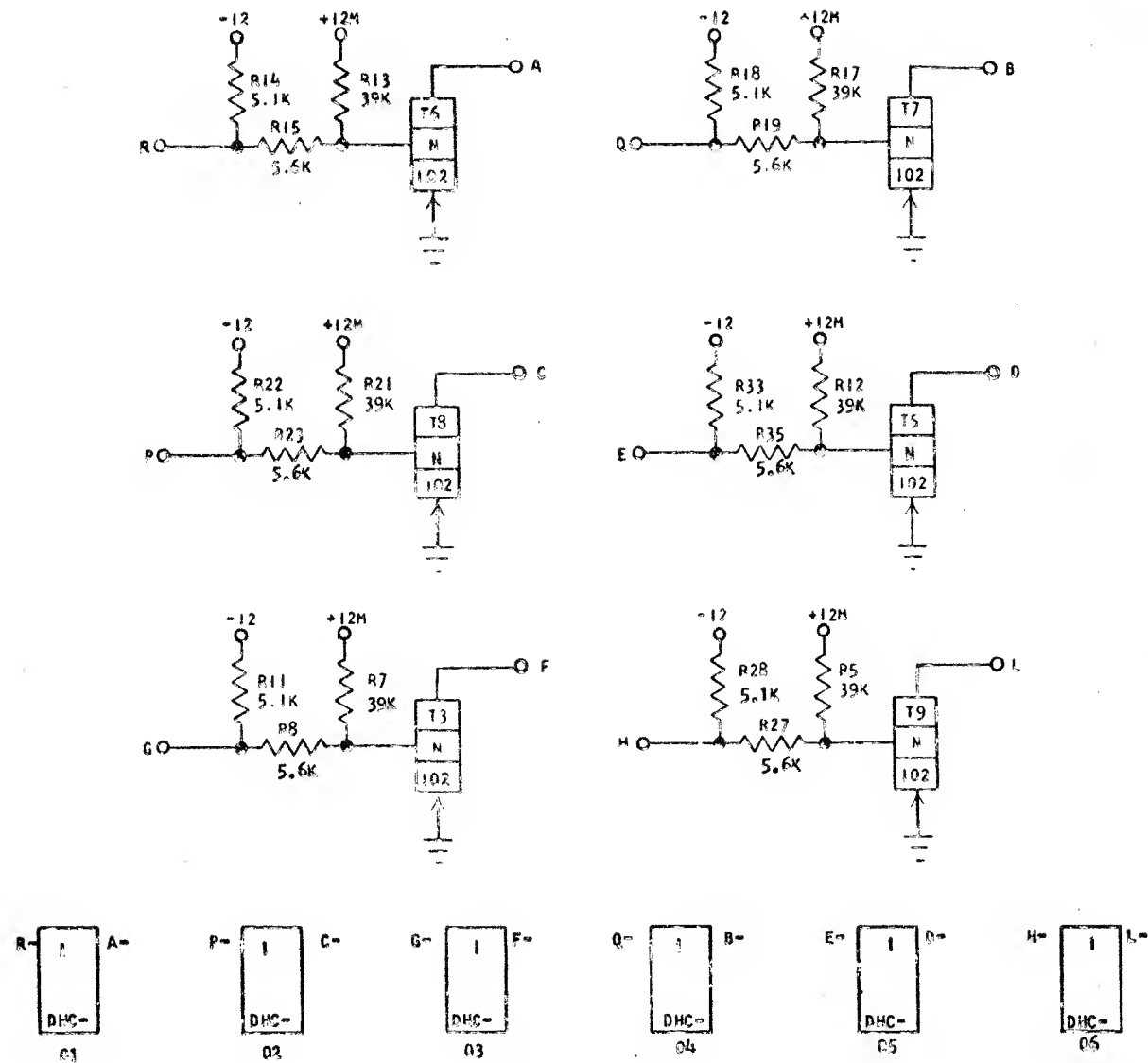
2157225

SDTDL INVERTER LOW SPEED W/O LOAD

1311

C2.90.25.0

DHC

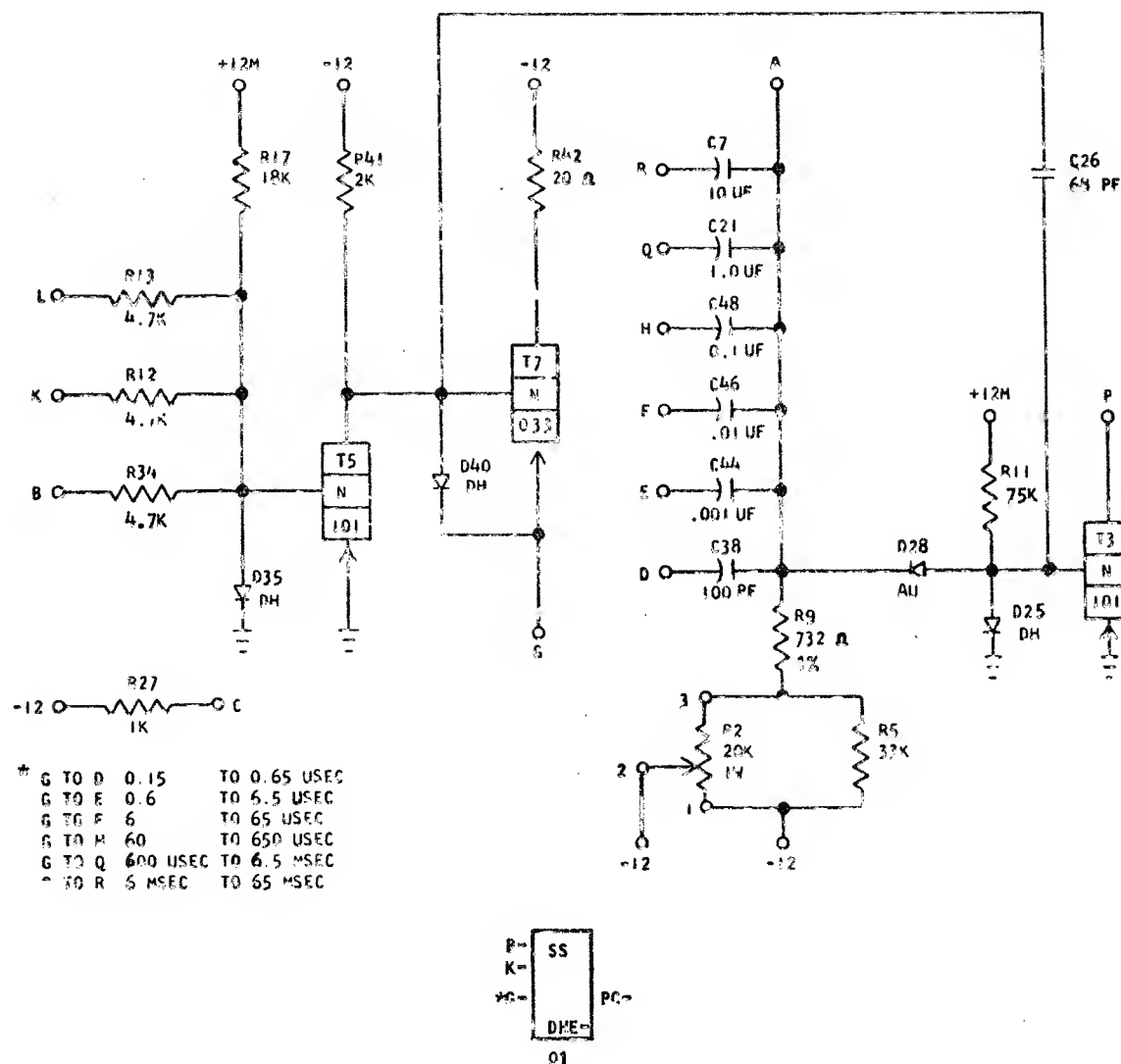


370372 REF

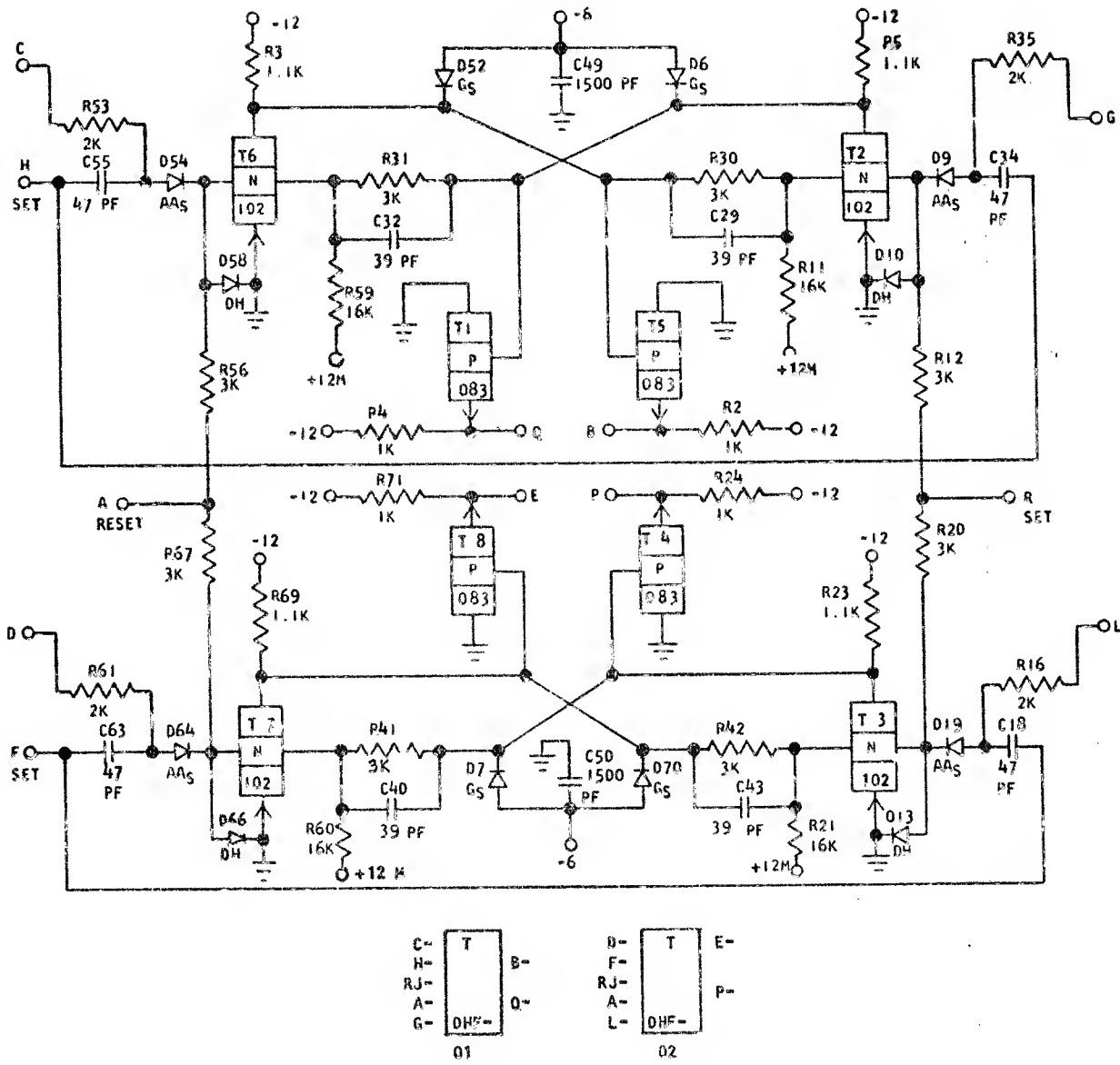
SDTDL - SINGLE SHOT

0.15 USEC TO 65 MSEC

DHE



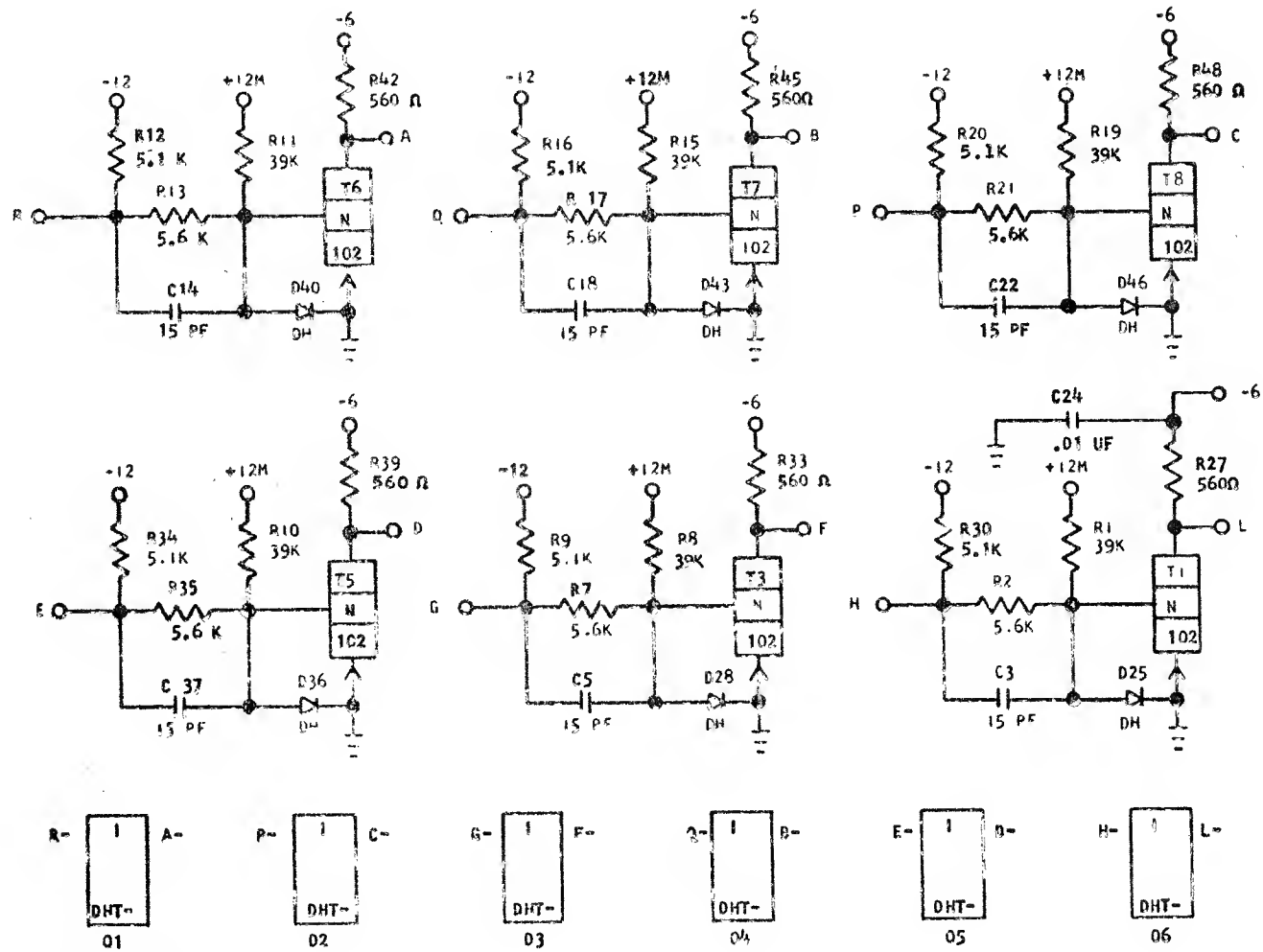
370262 REF



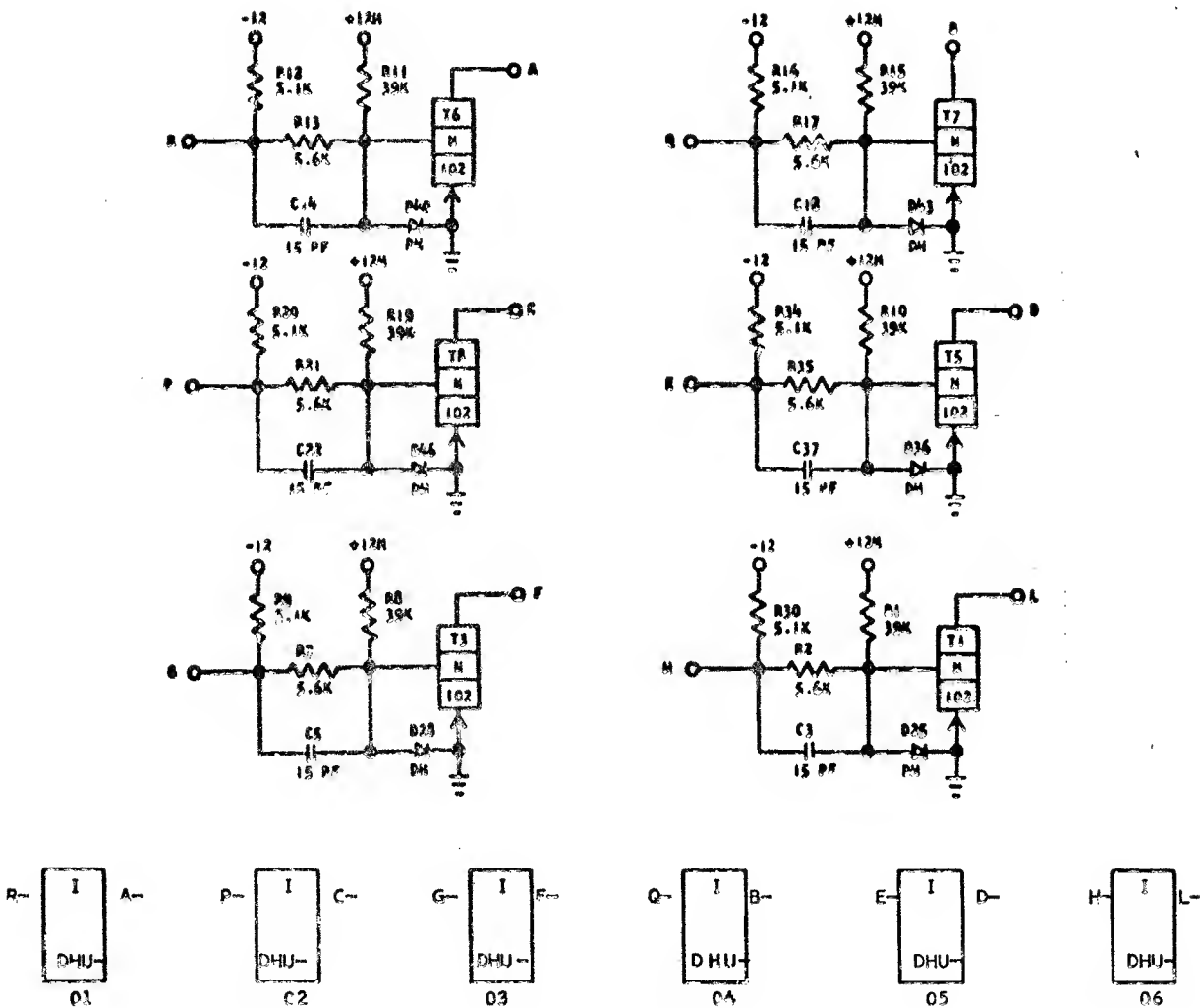
370350 REF

SDTDL-H.S. LOGIC INVERTER

DHT



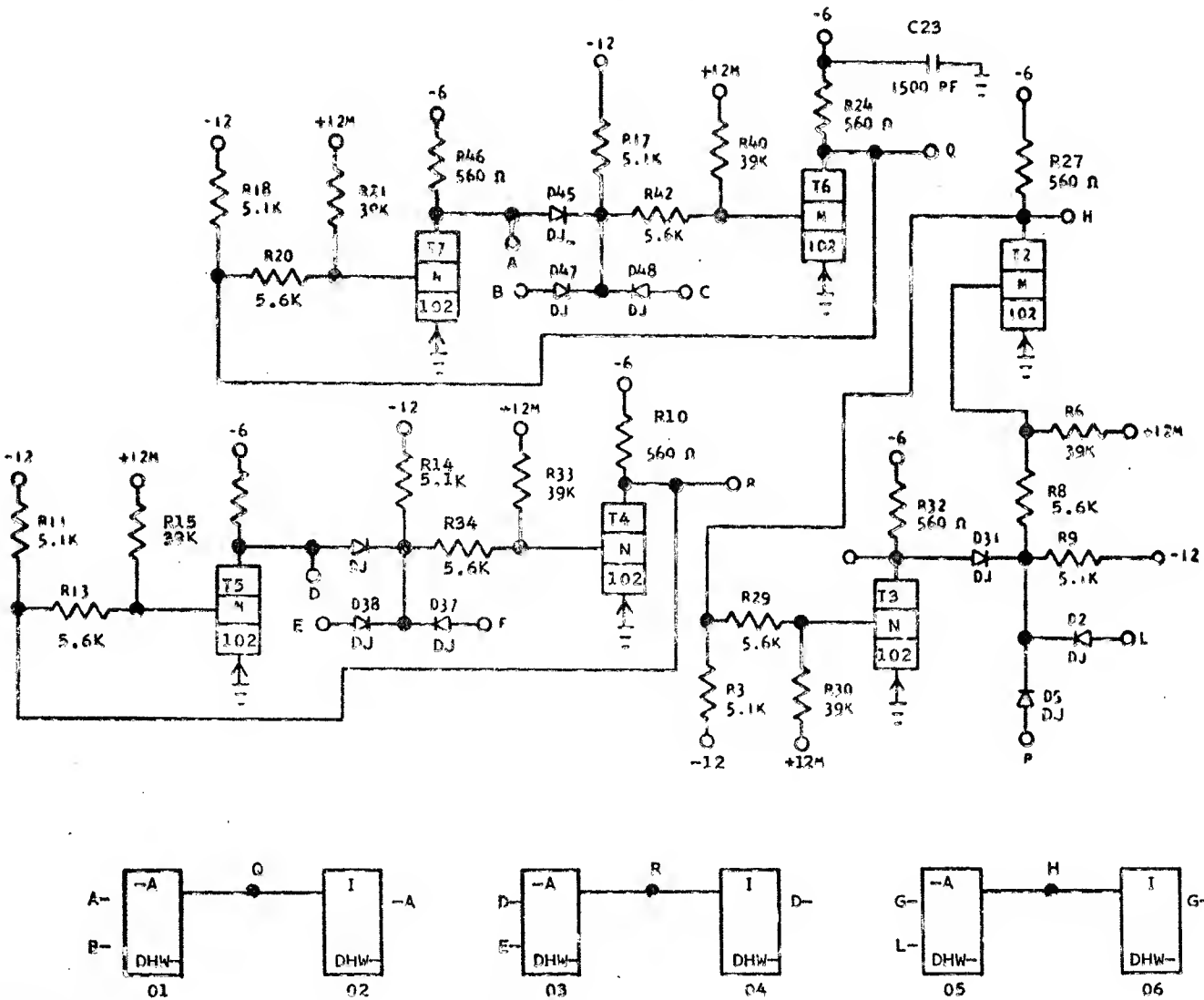
372168 REF



372169 REF

LATCH 3/CARD

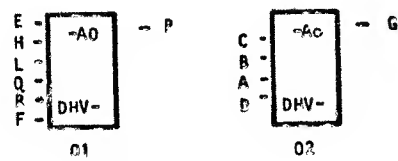
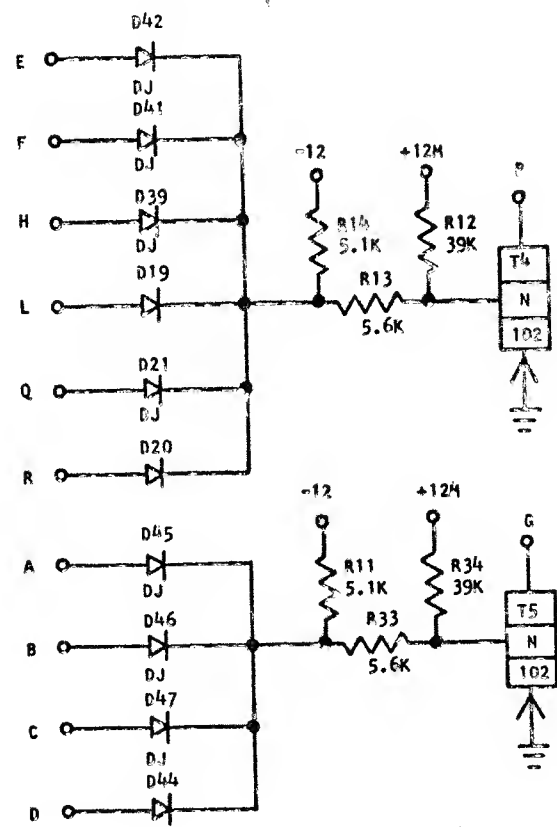
DHW



372191 REF

DHV-

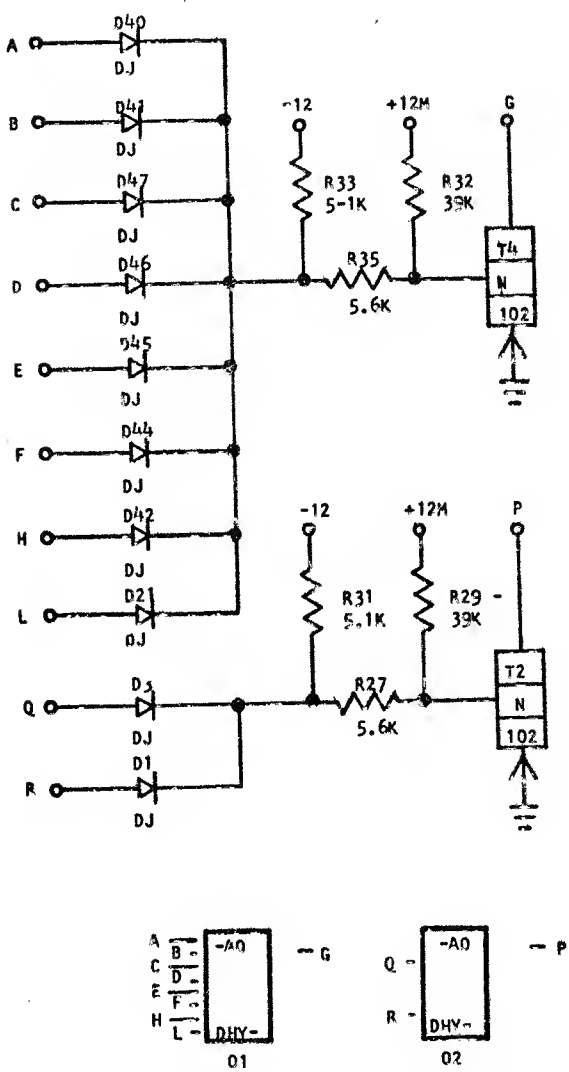
1 - 6 WAY, 1 - 4 WAY W/O LOAD (-A)



372123 REF

1 - 8 WAY, 1 - 2 WAY W/O LOAD

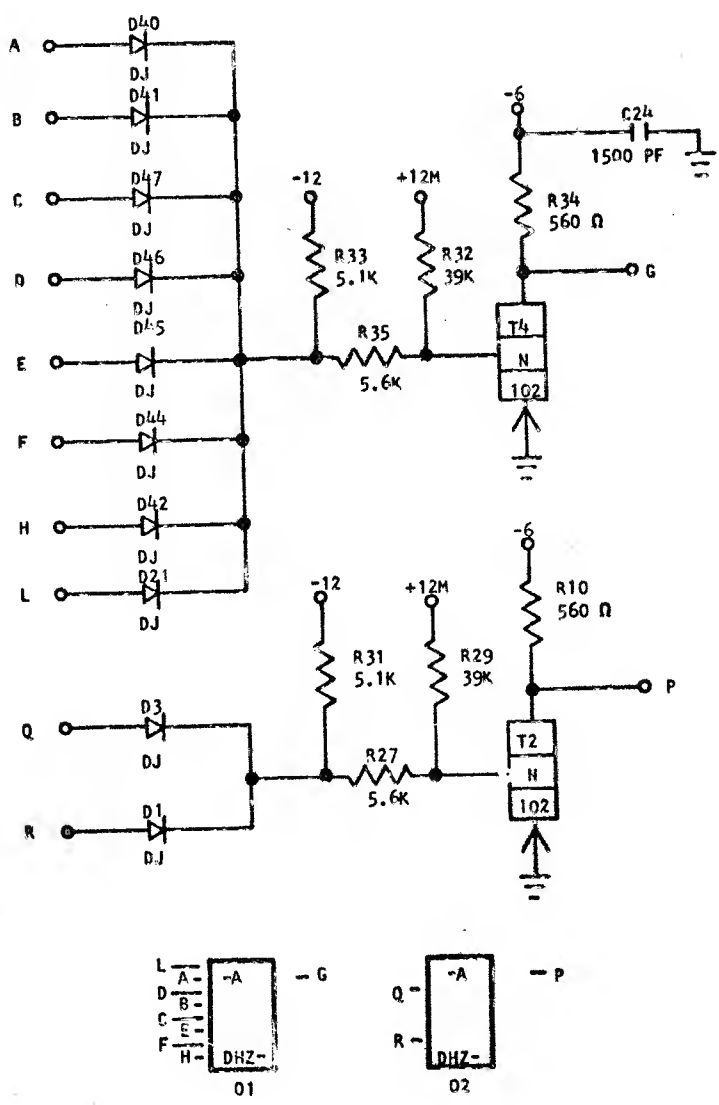
DHY-



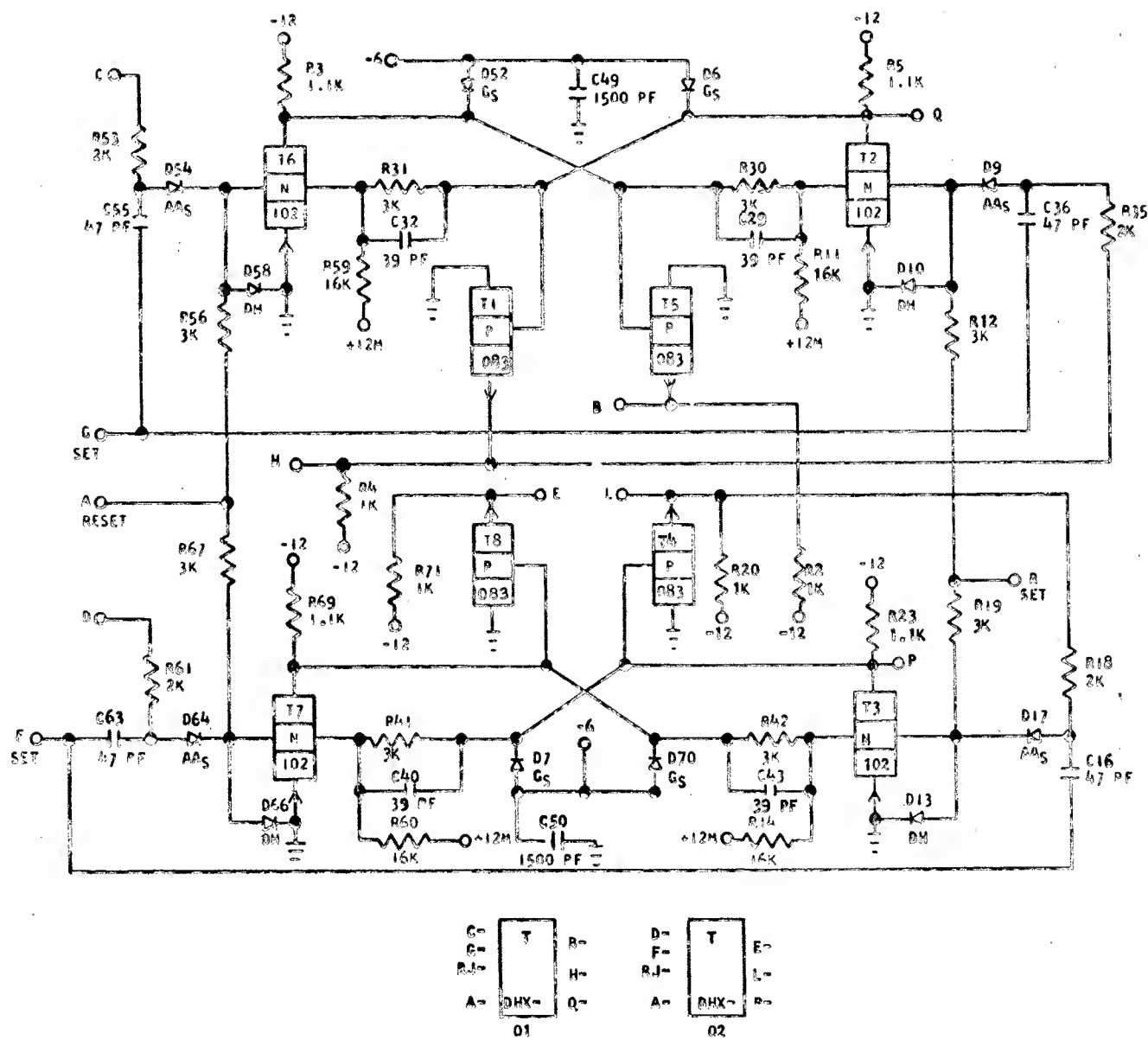
372193 REF

1 - 8 WAY AND 1 - 2 WAY W/LOAD

DHZ-



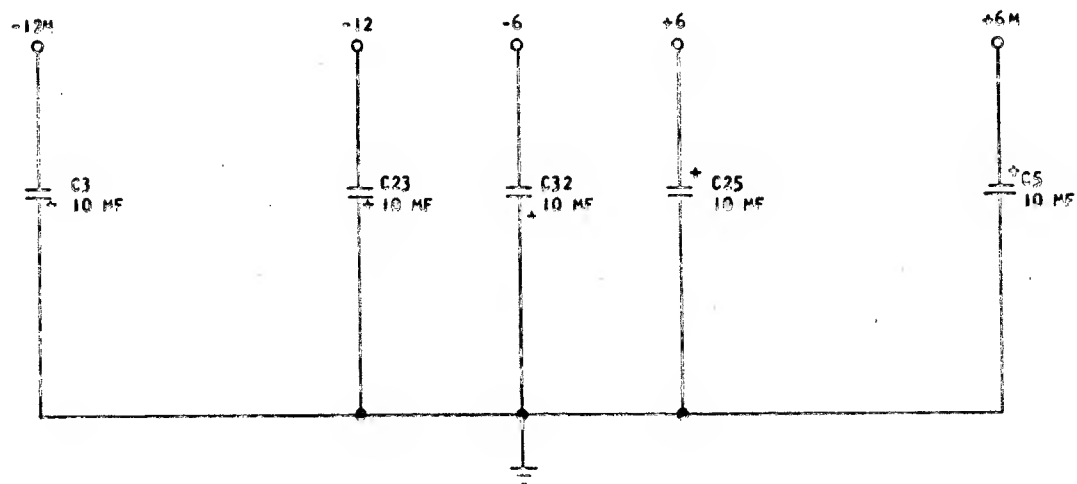
372194 REF



372192 REF

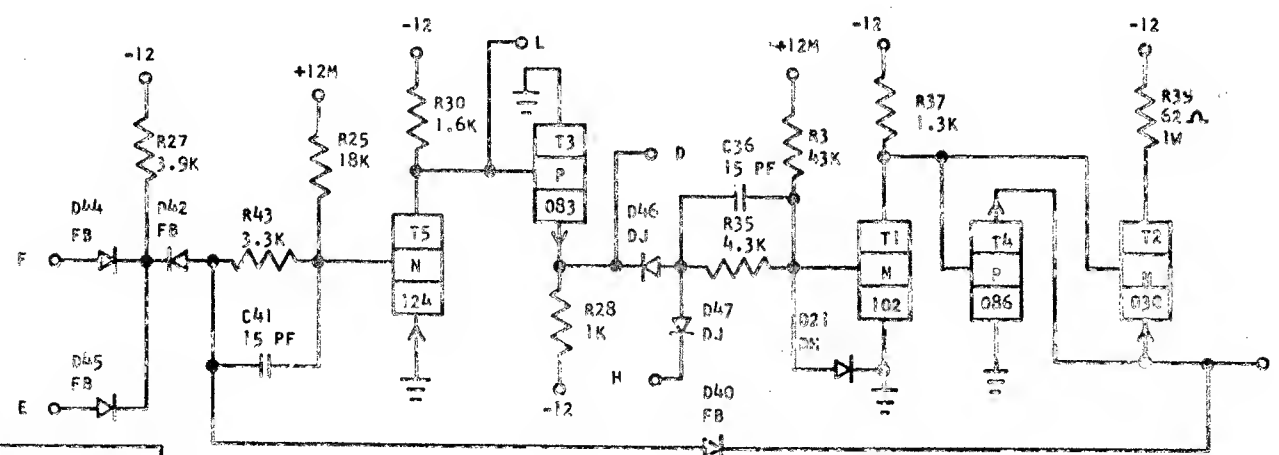
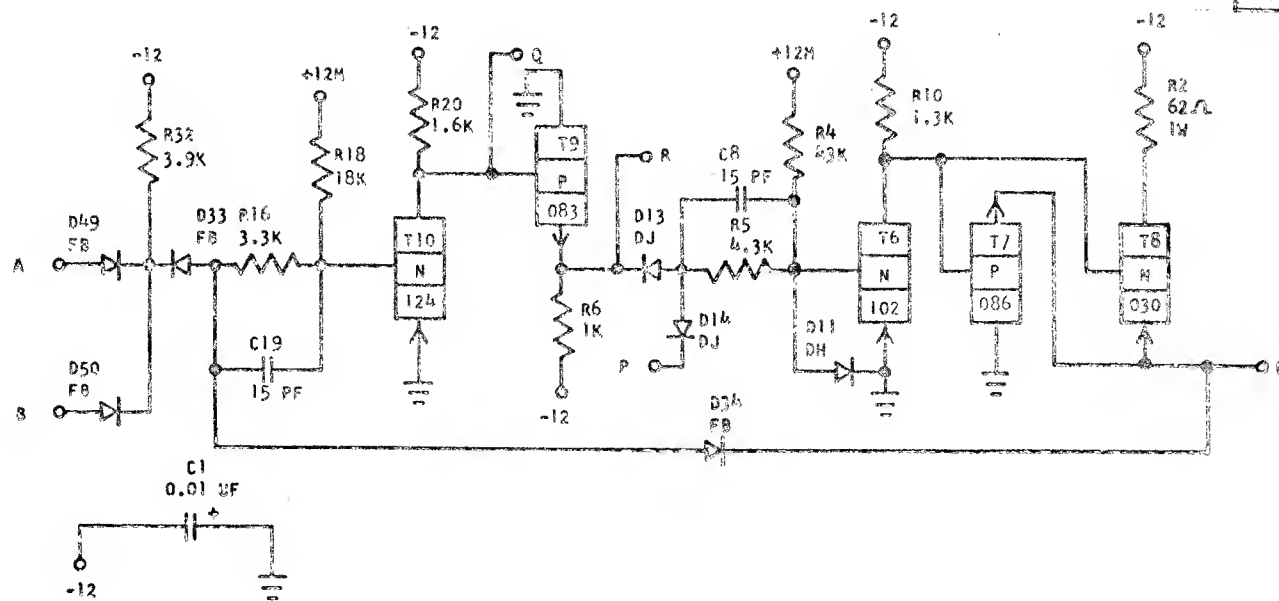
GENERAL PURPOSE FILTER CARD

GJ

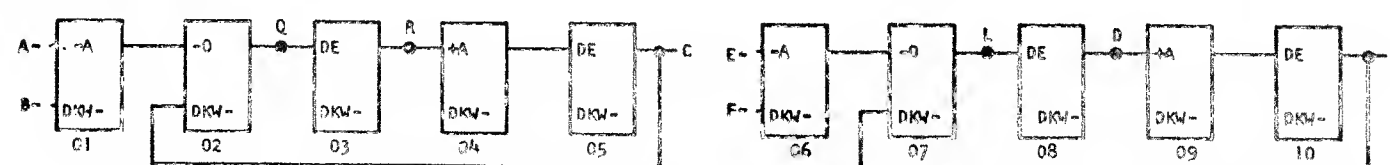


371501 REF

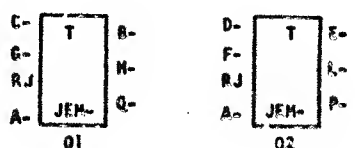
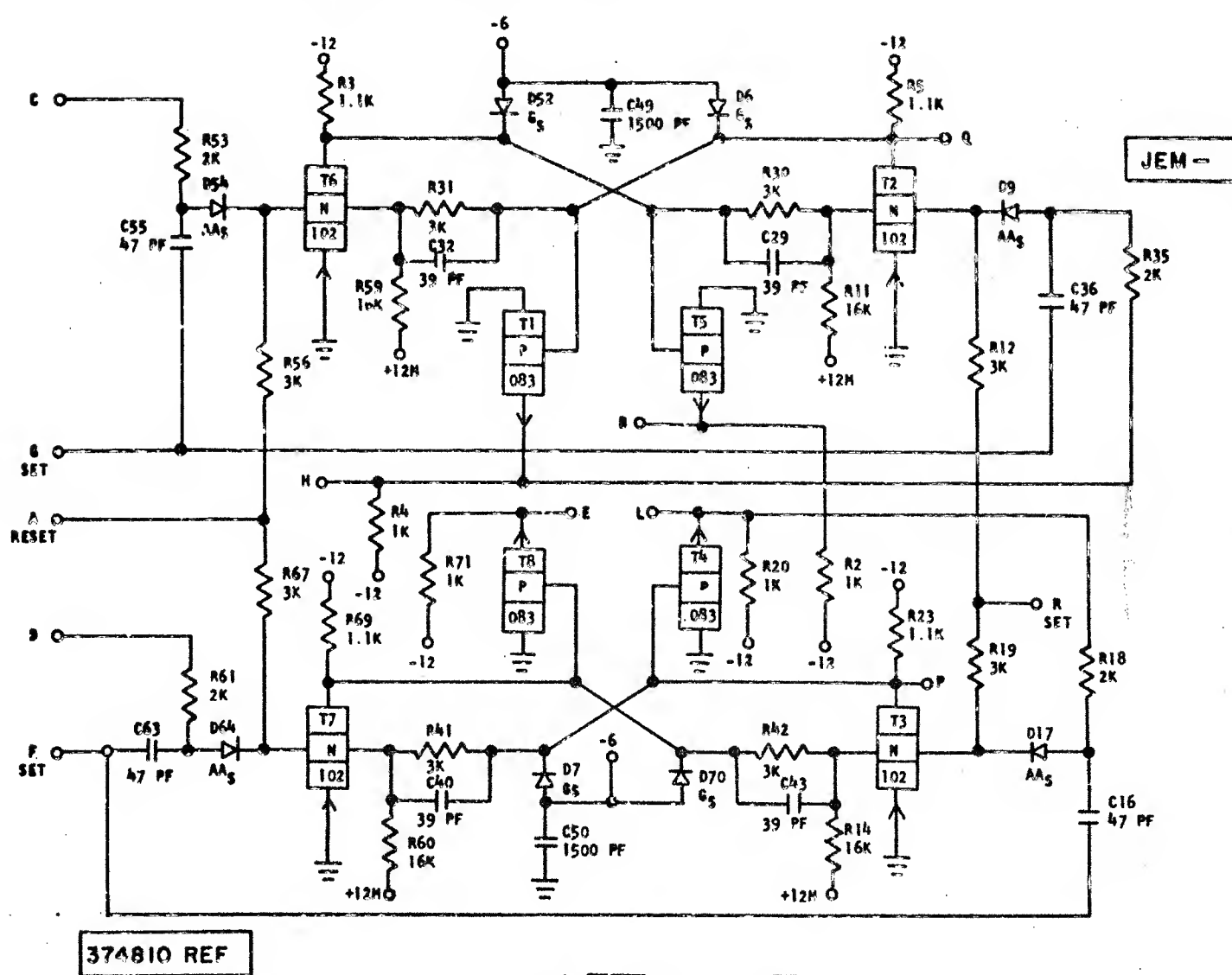
DKW-



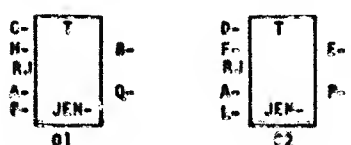
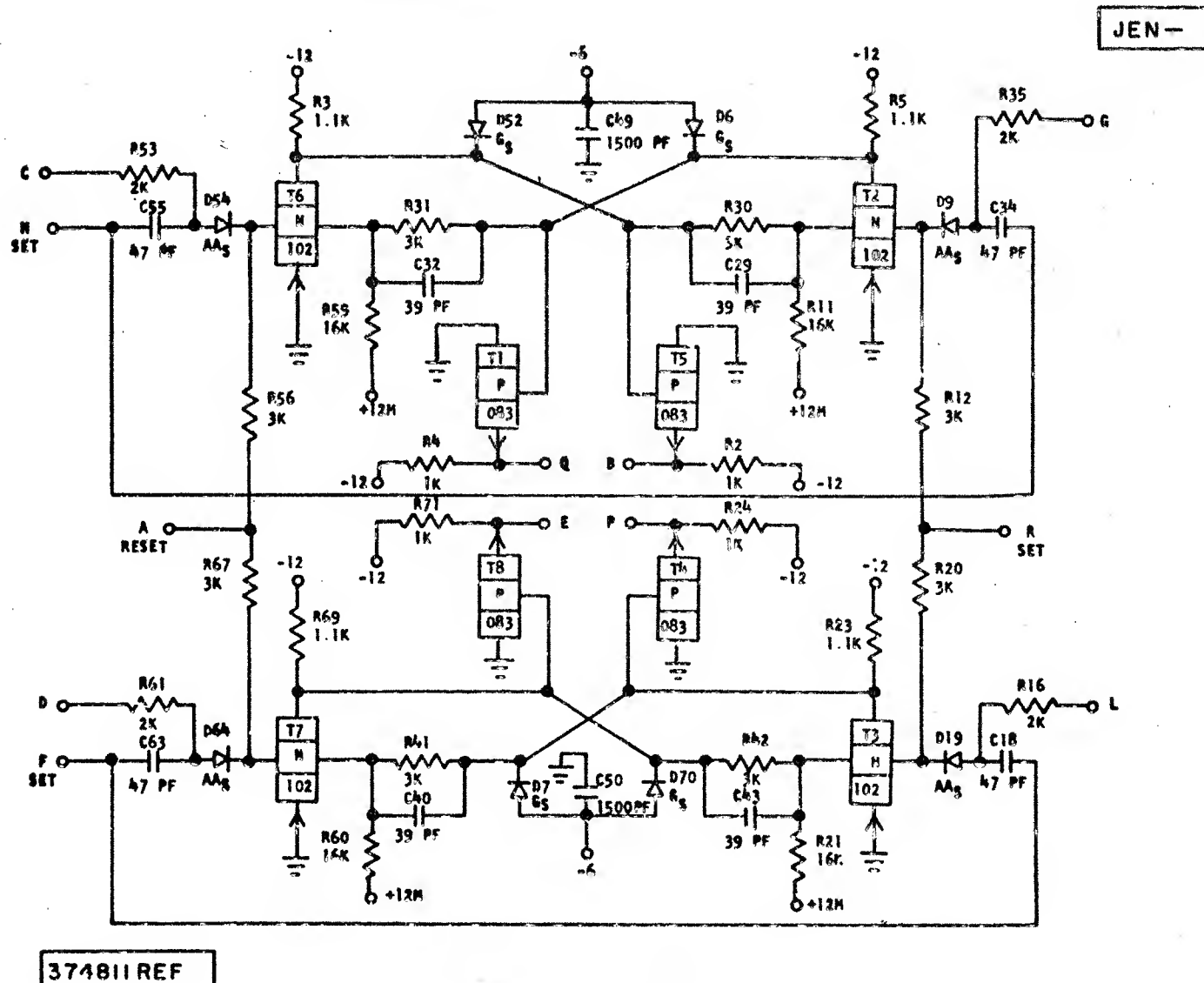
372526 REF

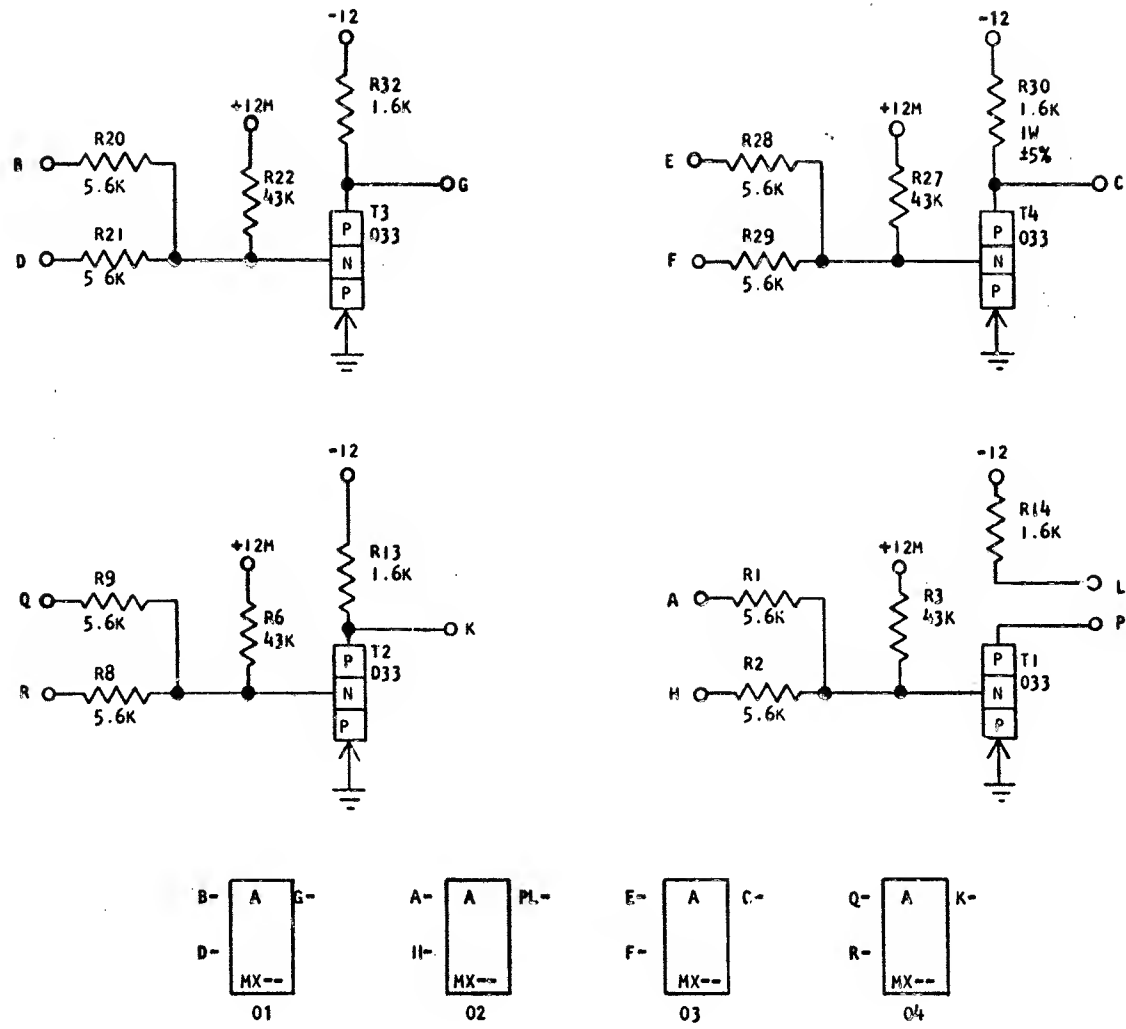


BINARY PULLOVER TRIGGER



SDTDL TRIGGER AND DRIVER

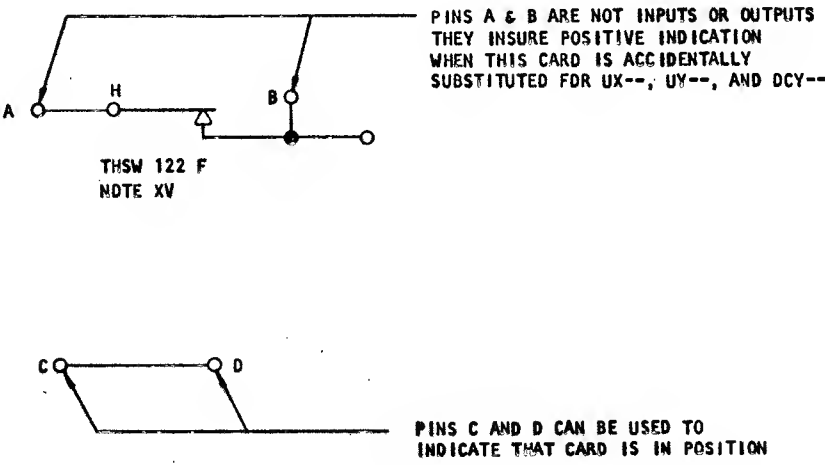




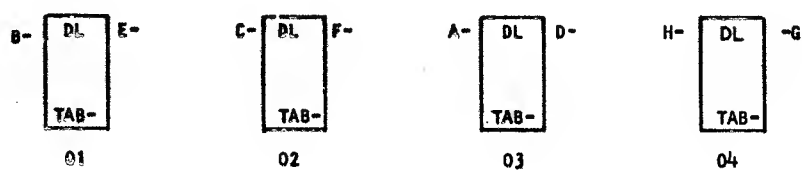
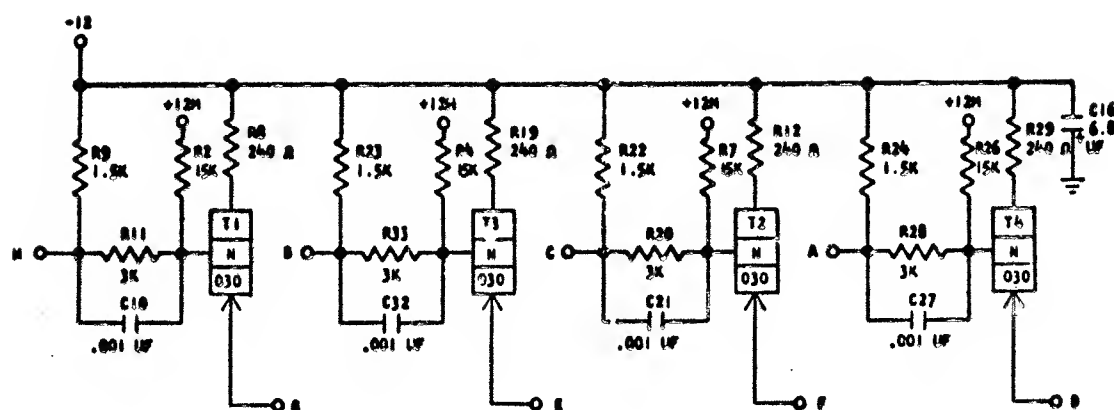
371661 REF

ALLOY-THERMOSWITCH N/C 122°F

RE--



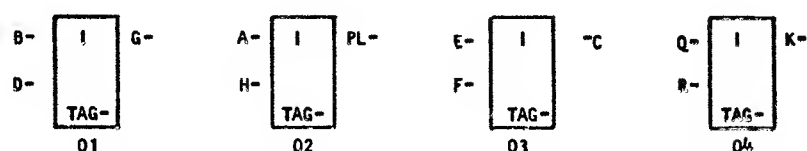
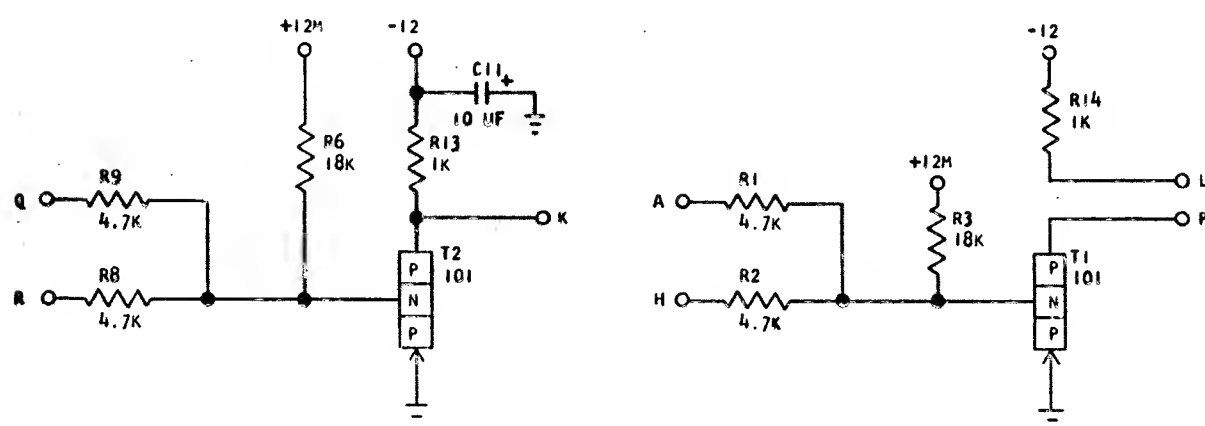
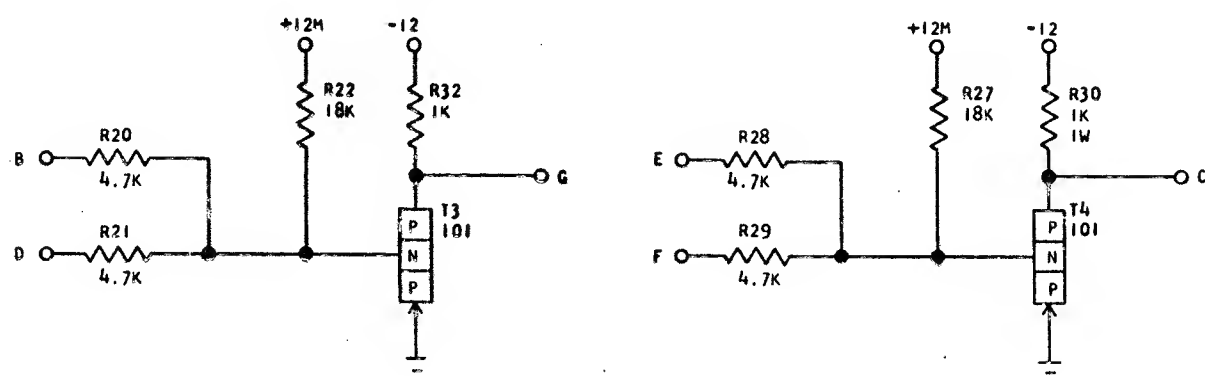
371699 REF



370066 REF

SDTRL-2 WAY INVERTER

TAG



370366 REF

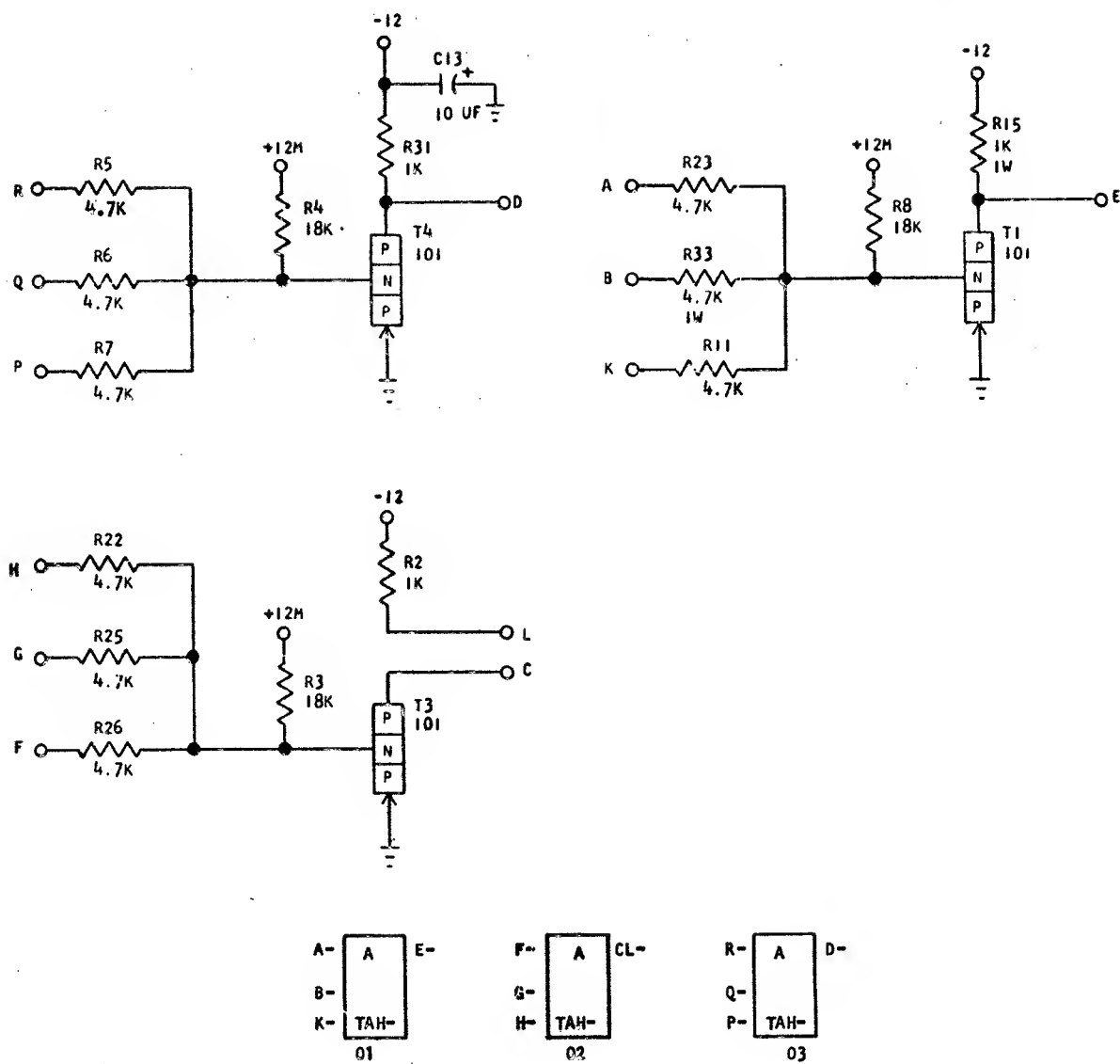
2157231

SDTRL - 3 WAY INVERTER

1311

C2.90.31.0

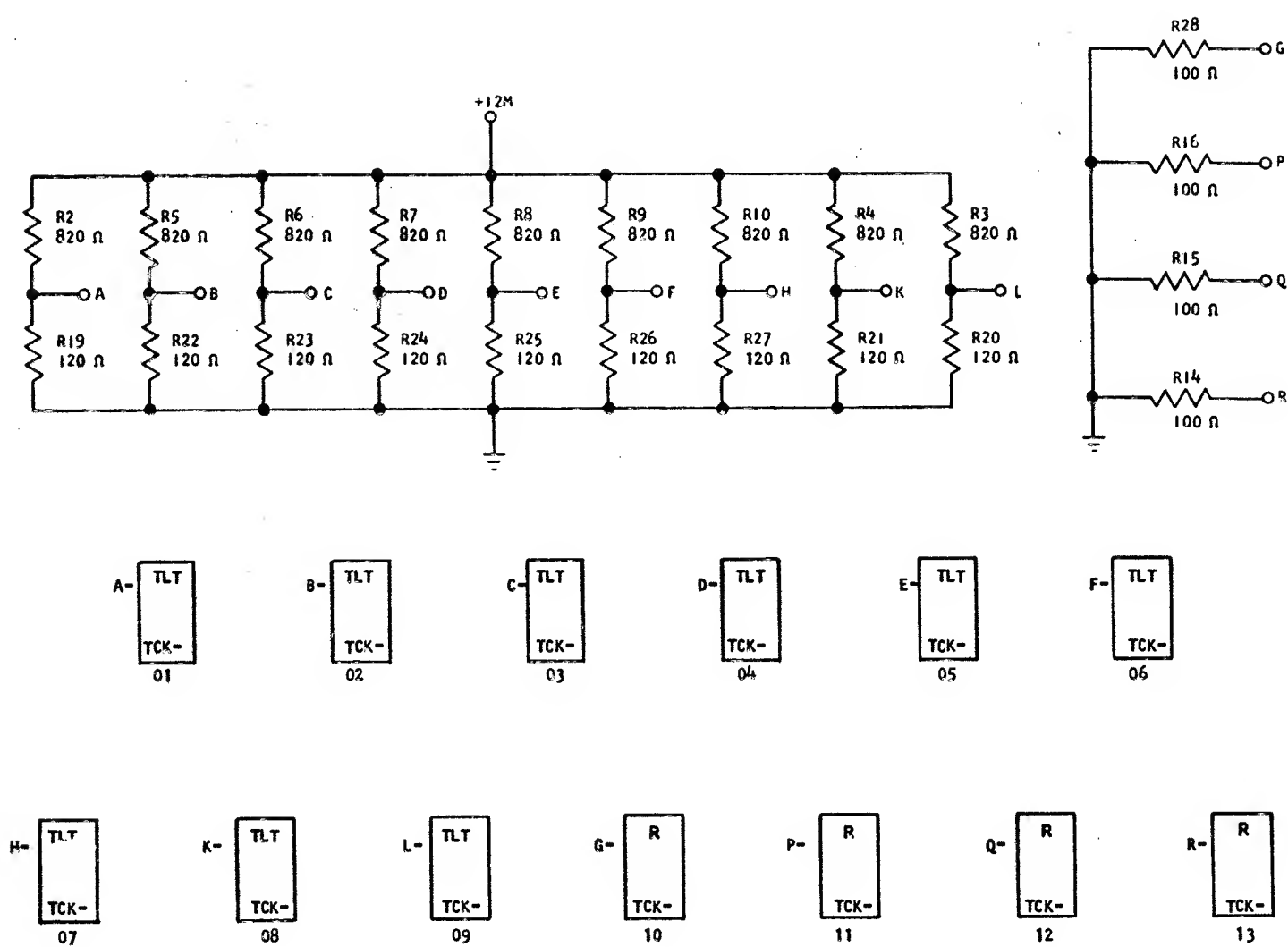
TAH



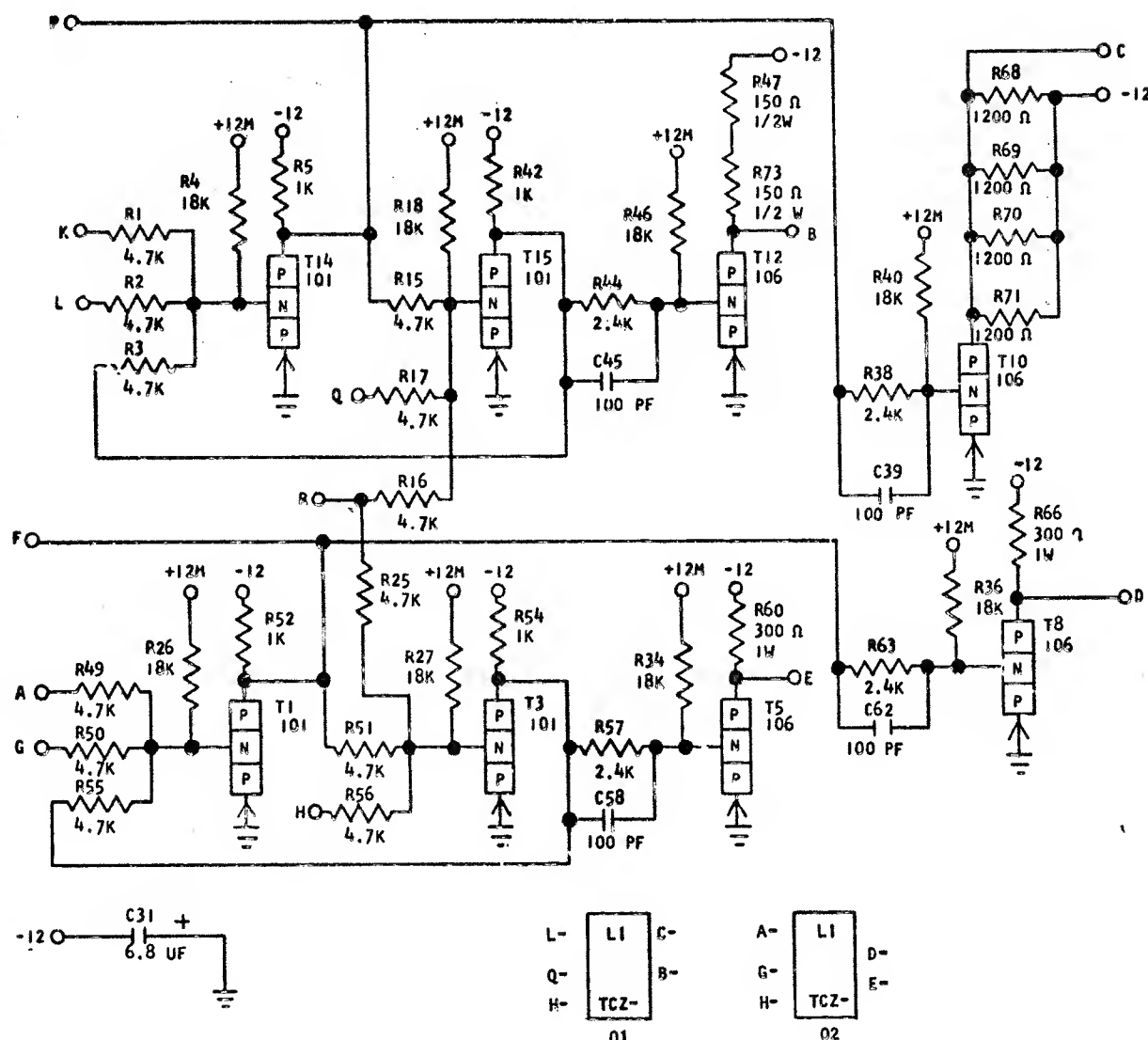
370367 REF

SDTRL - END OF LINE TERMINATORS

TCK



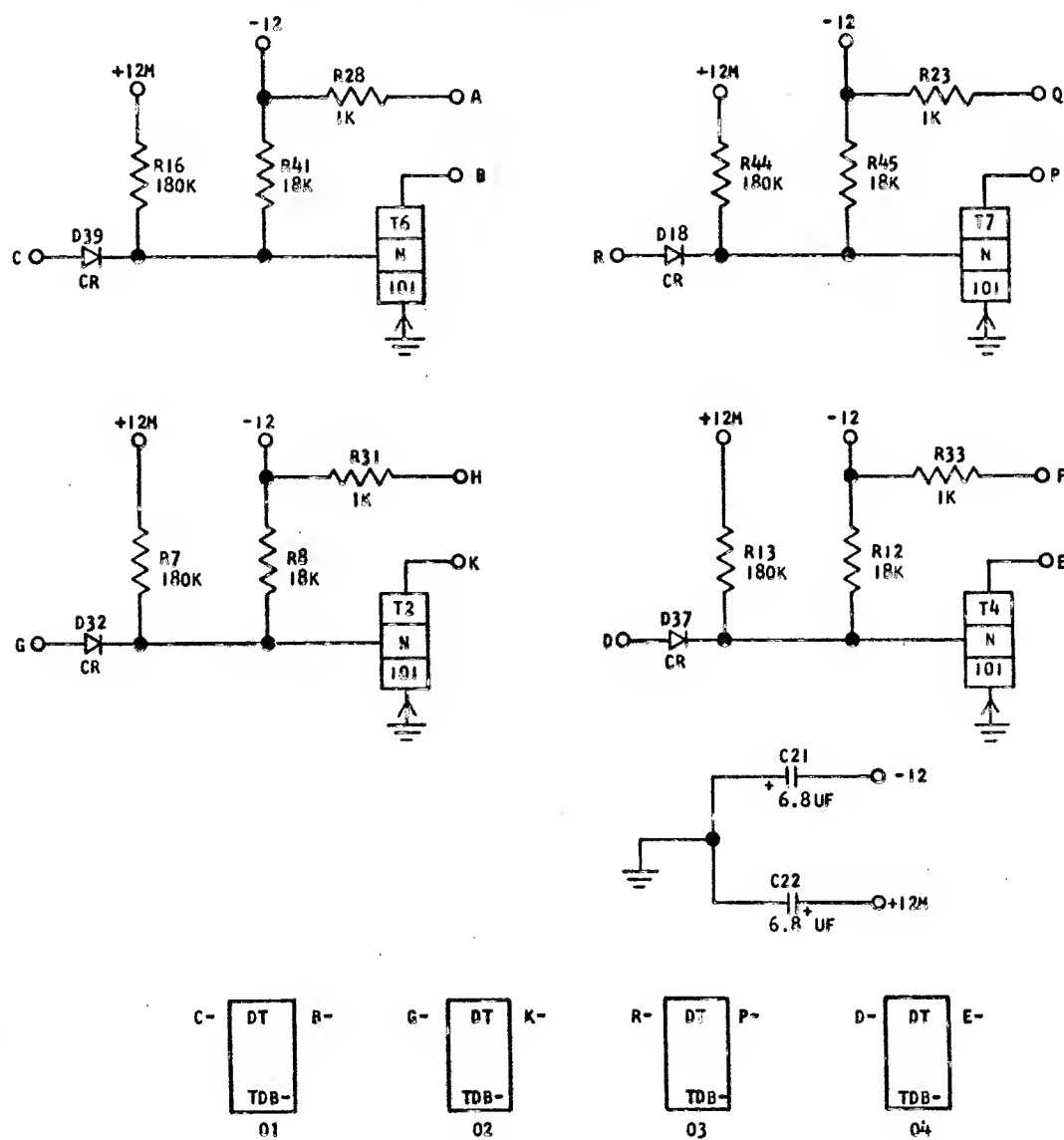
370334 REF



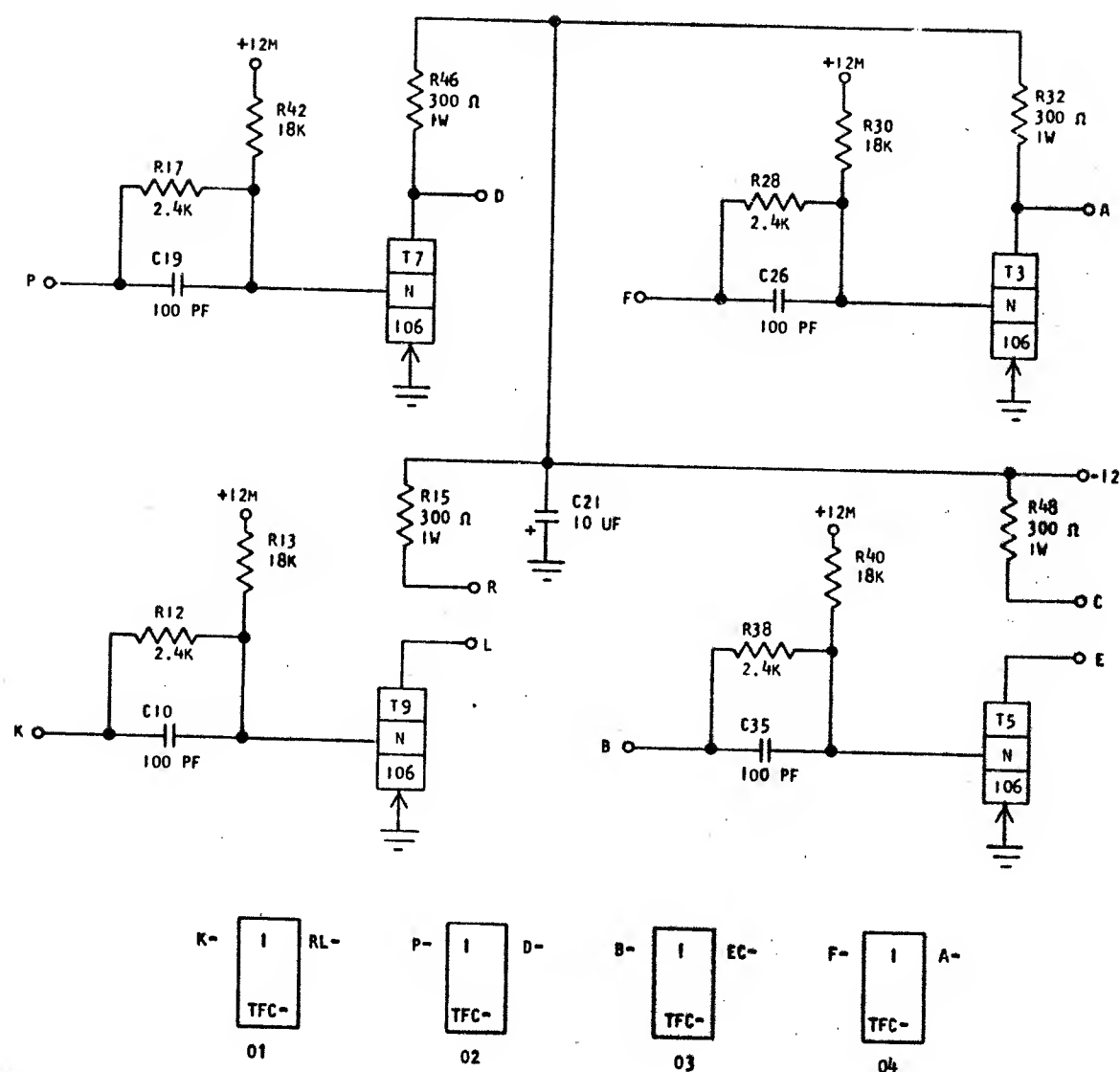
370335 REF

SDTRL-DISTRIBUTED LINE TERMINATOR
WITH OPTIONAL LOAD RESISTORS

TDB



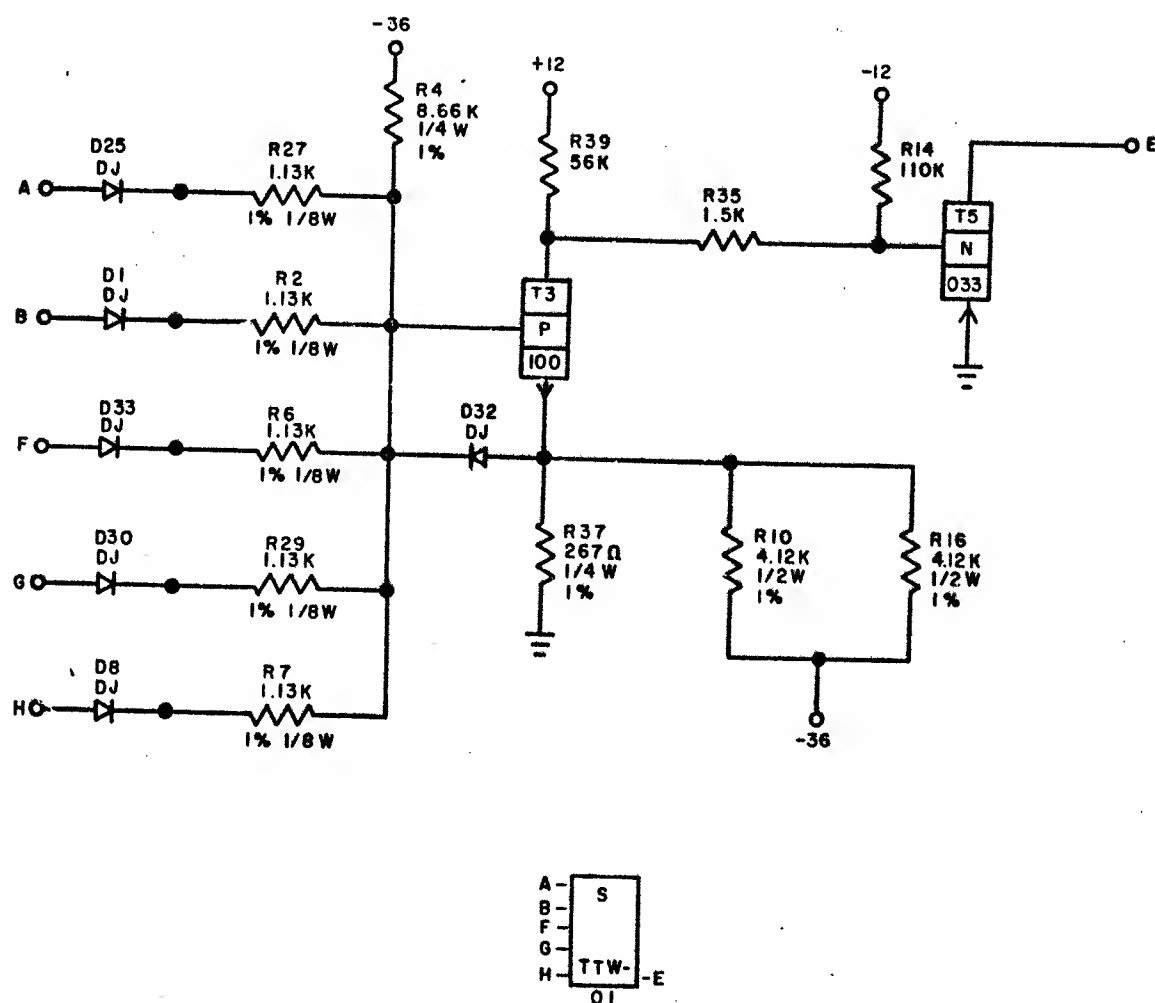
370389 REF



370646 REF

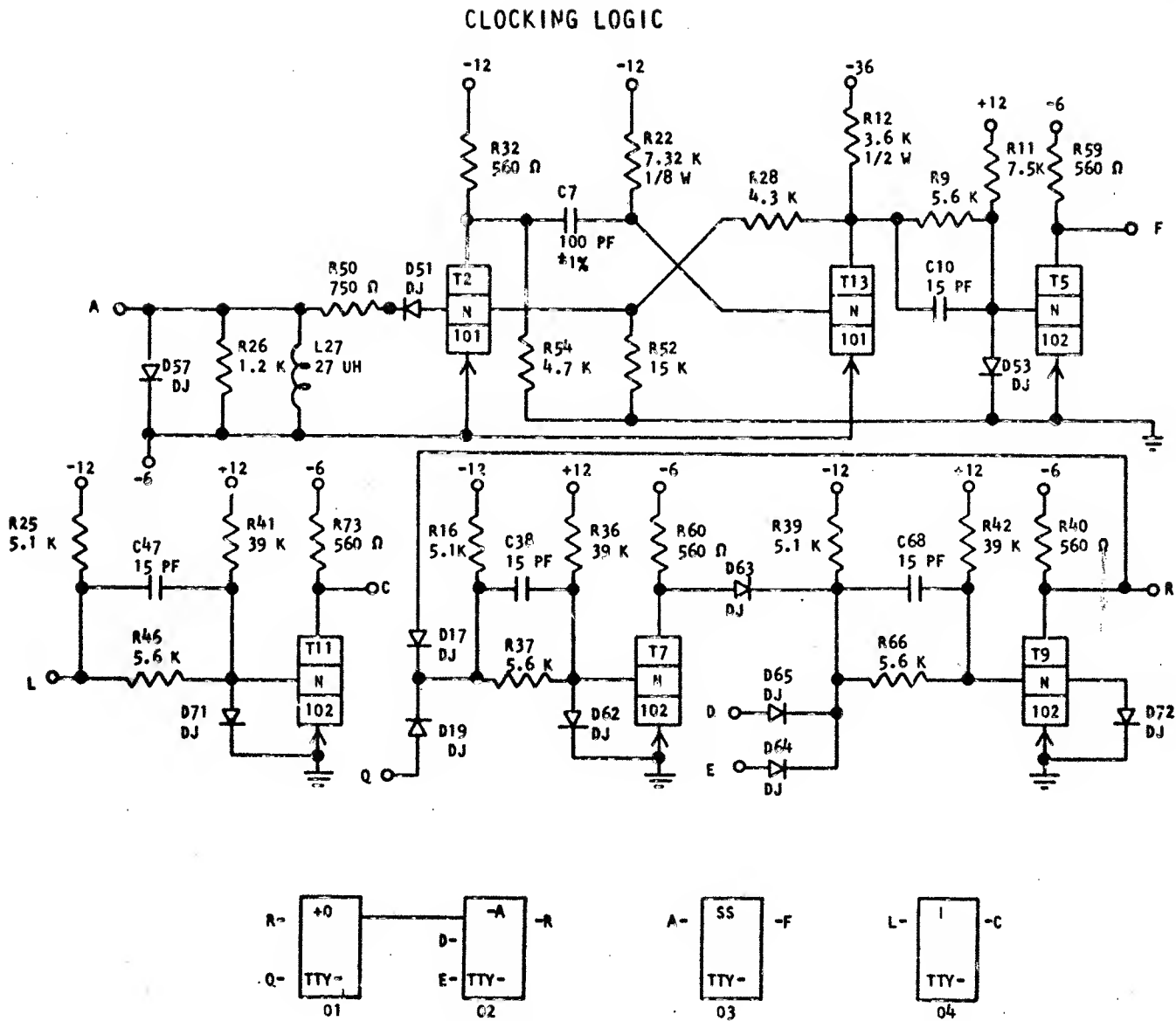
MODULE SELECT SAFETY

TTW-



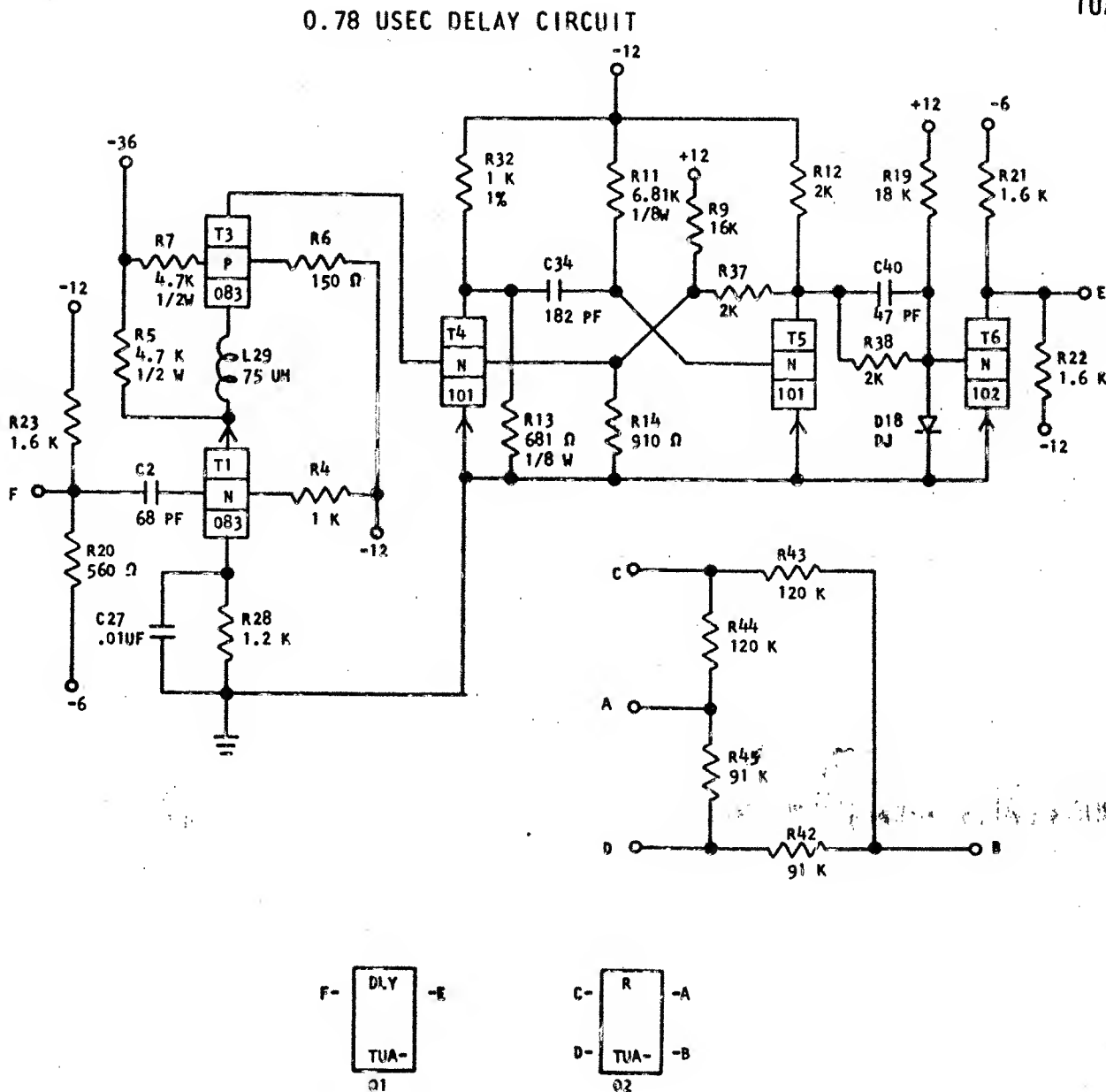
372542 REF

TTY-



372544 REF

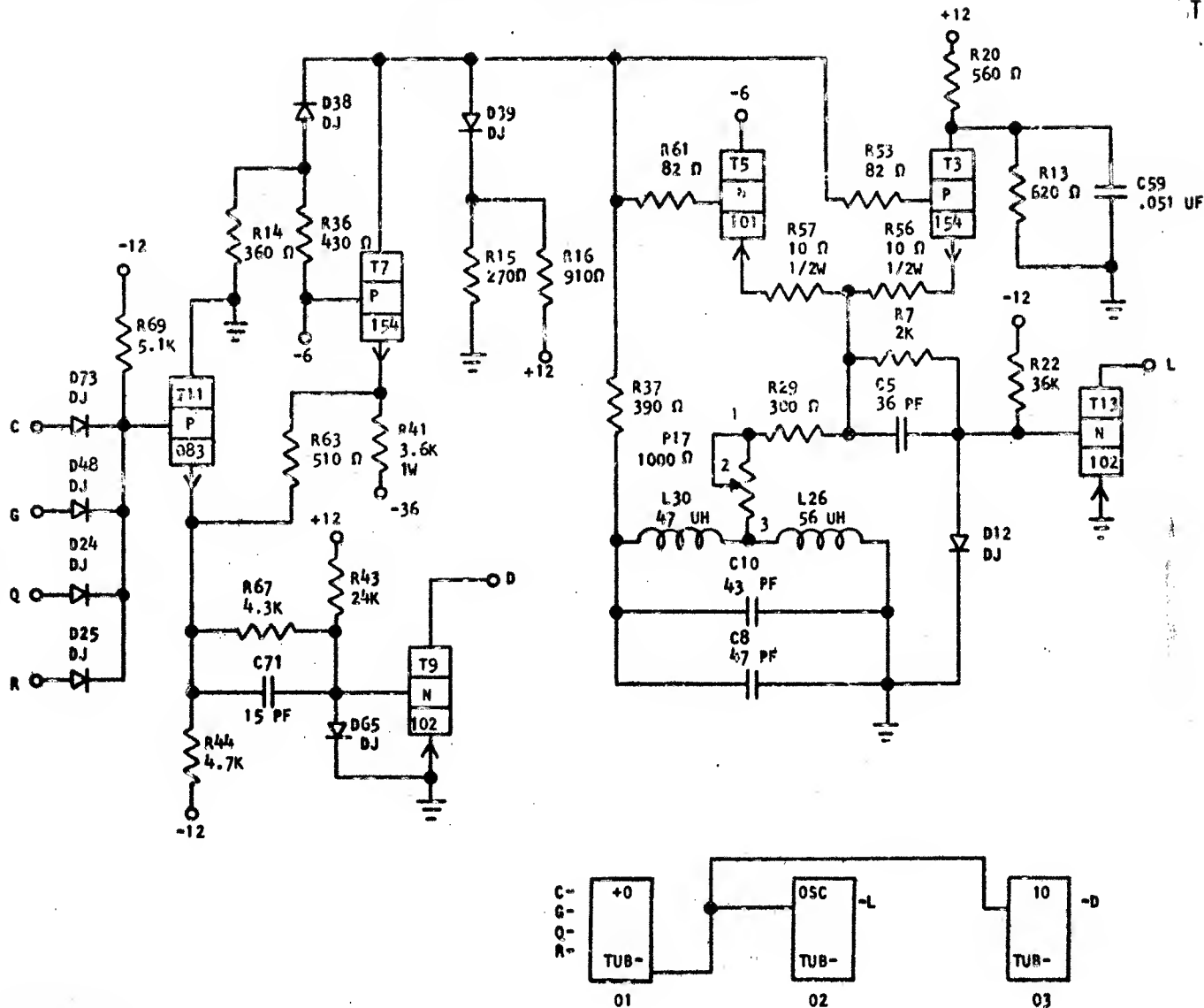
TUA-



372547 REF

1.399 MC GATED OSCILLATOR

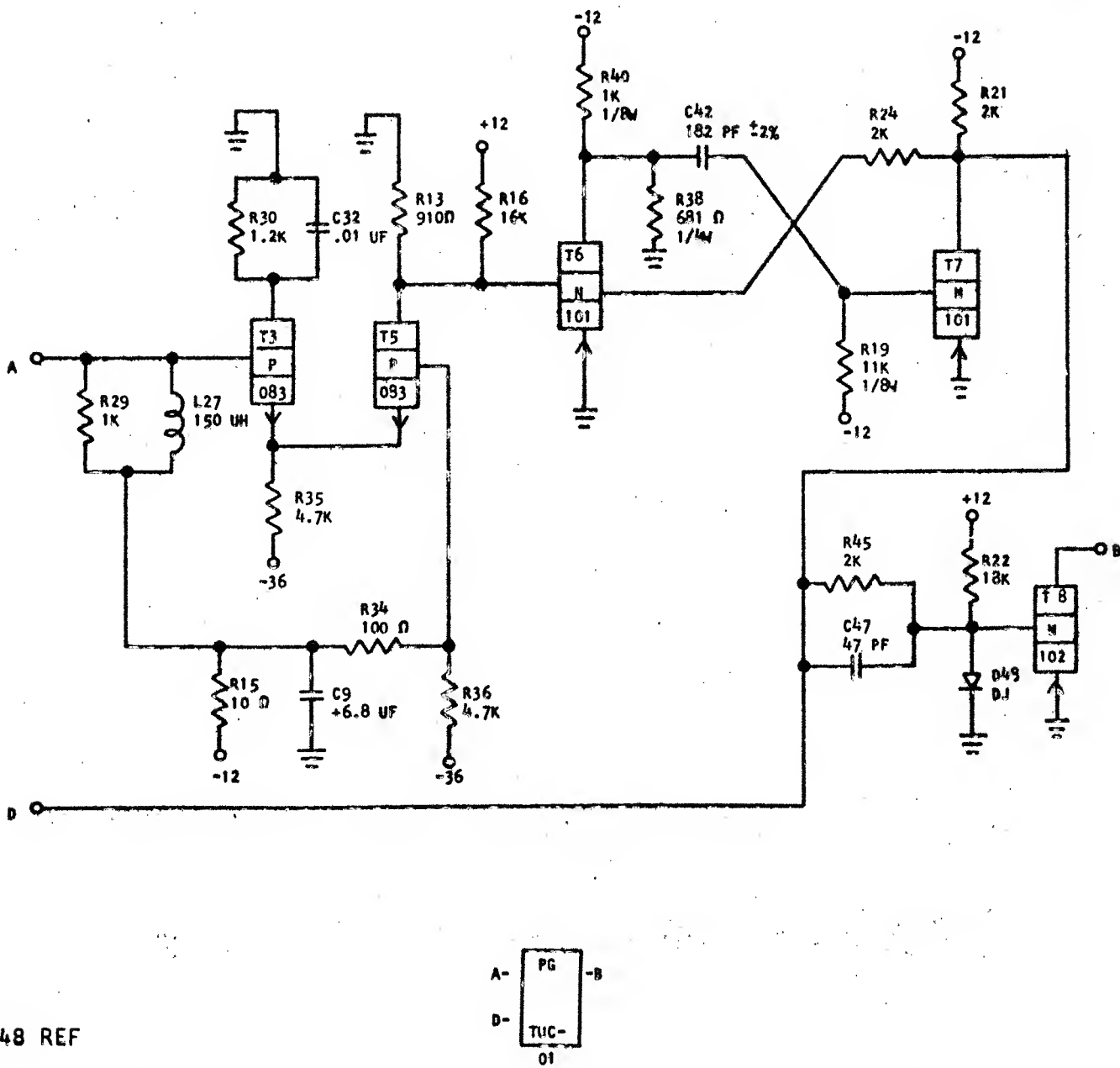
TUB-



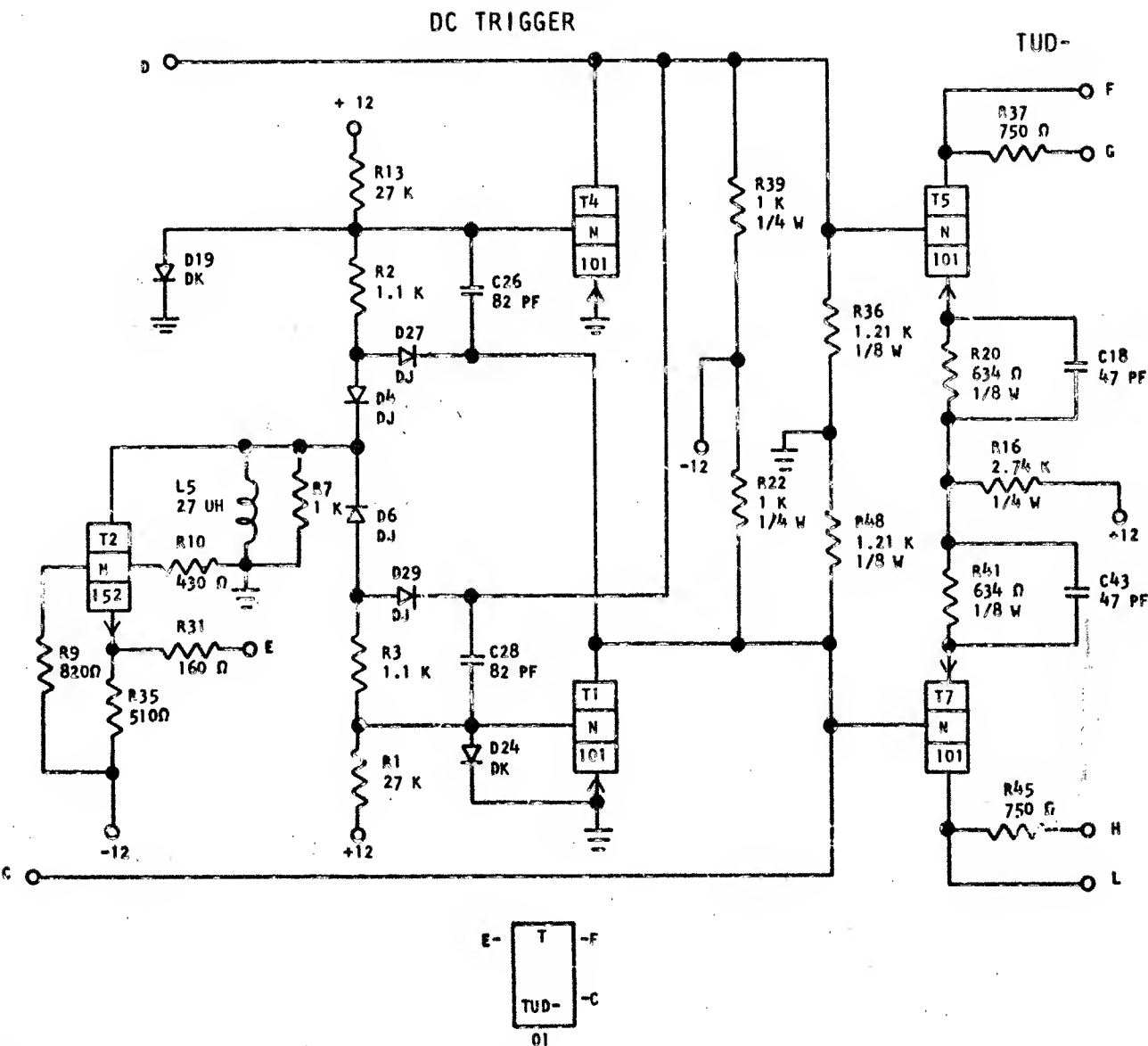
372549 REF

DETECTOR AND SINGLE SHOT #2

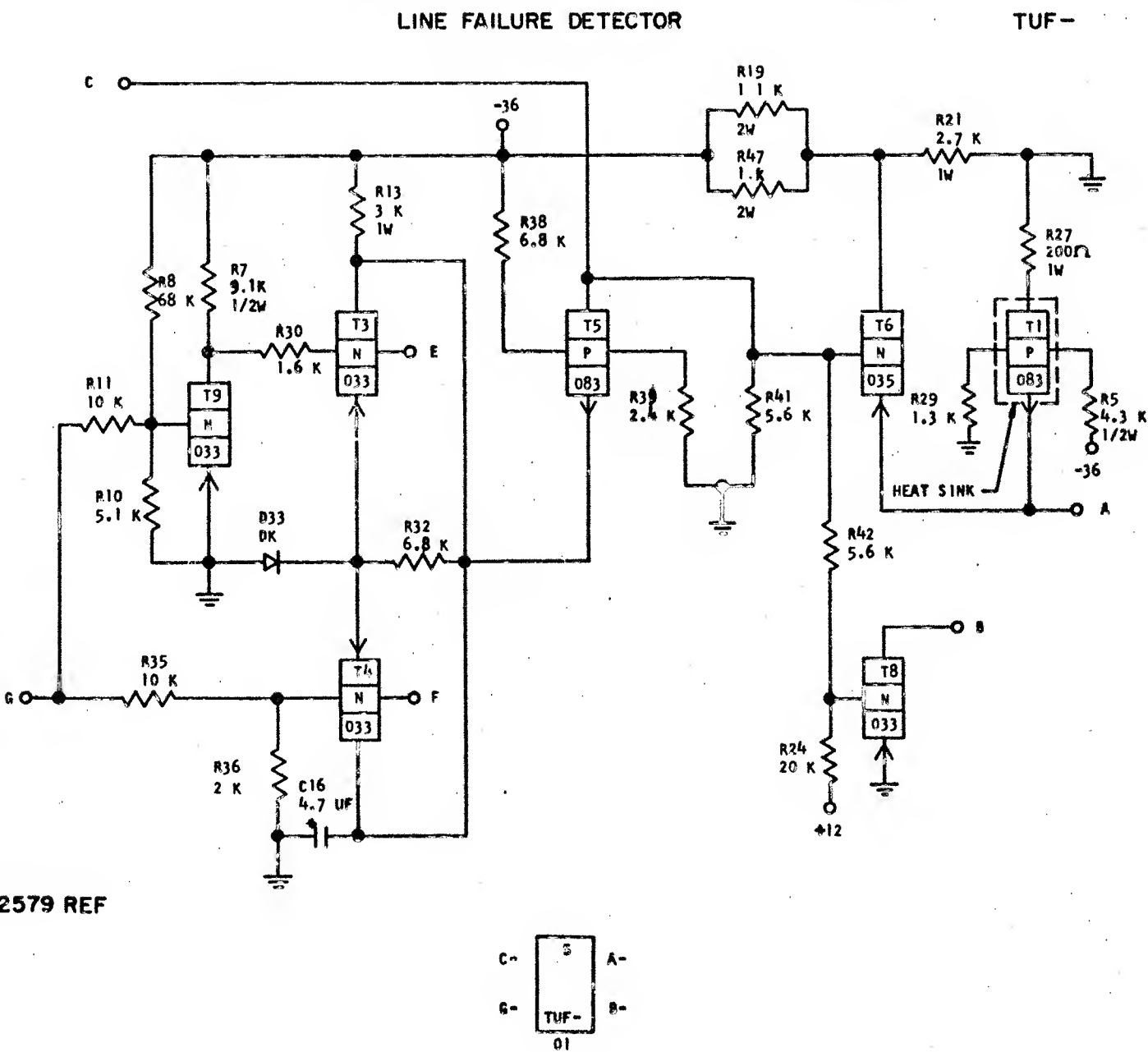
TUC-



372548 REF

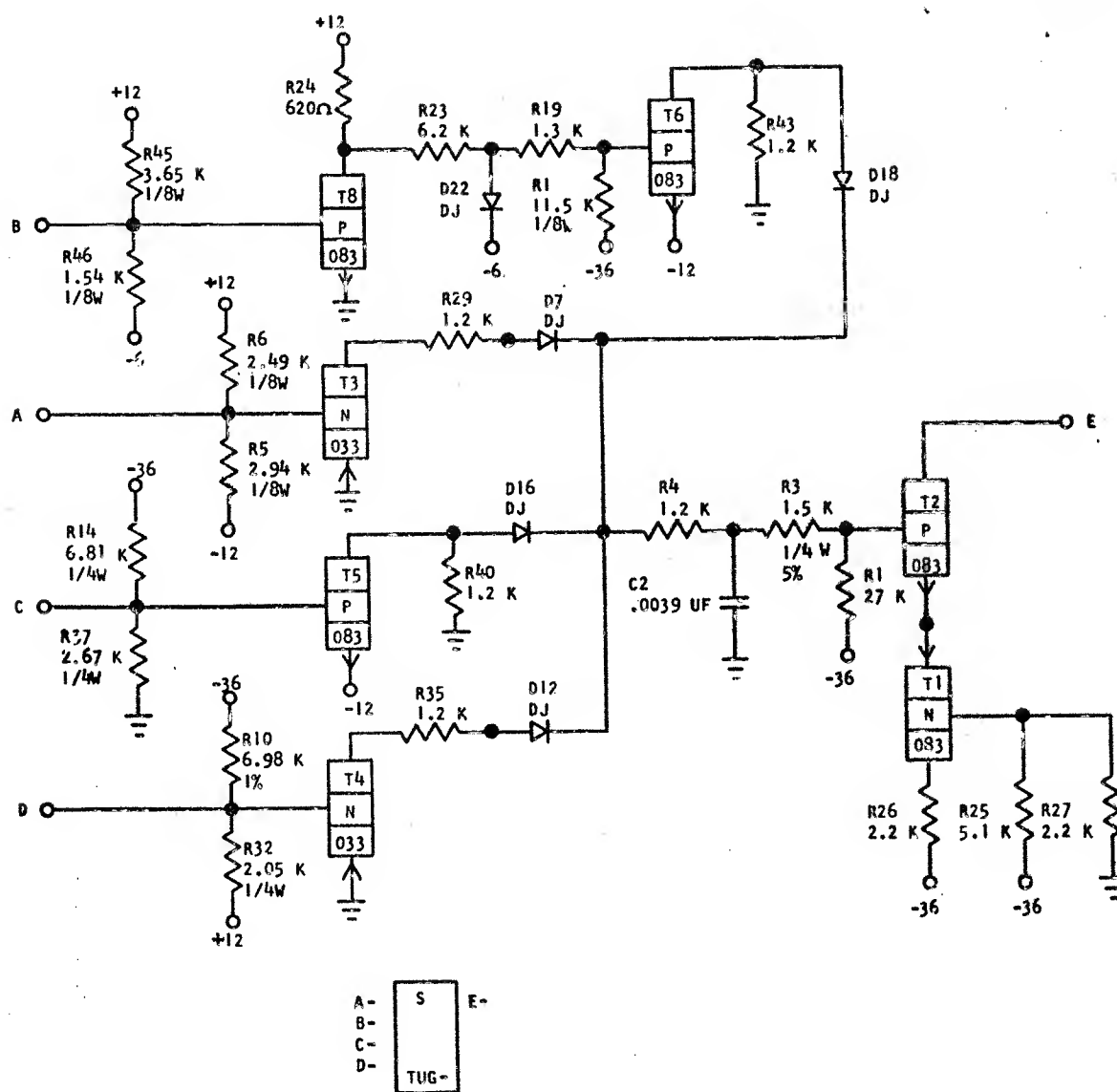


372546 REF



372579 REF

TUG-

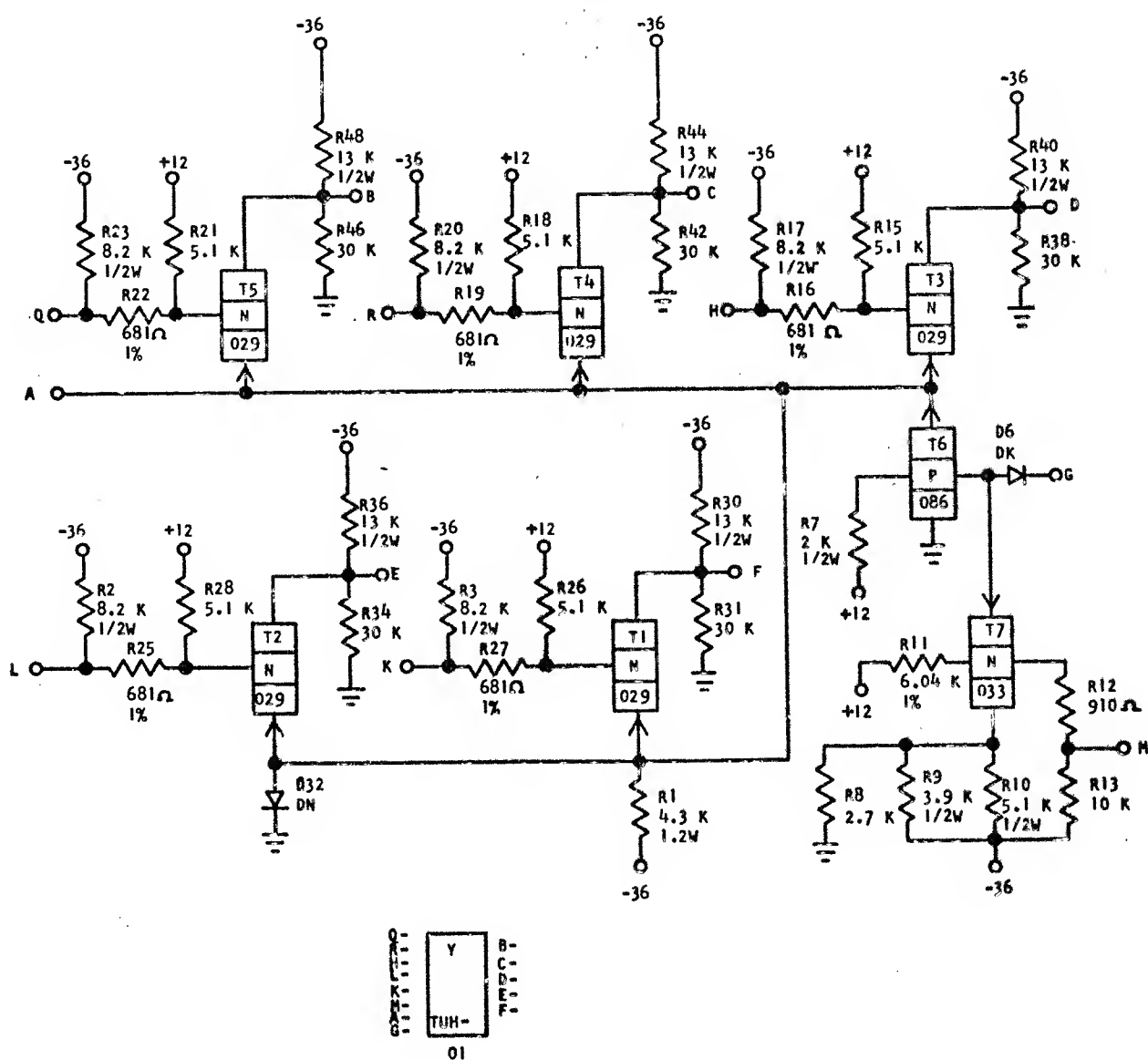


372578 REF

Y-SELECT #1

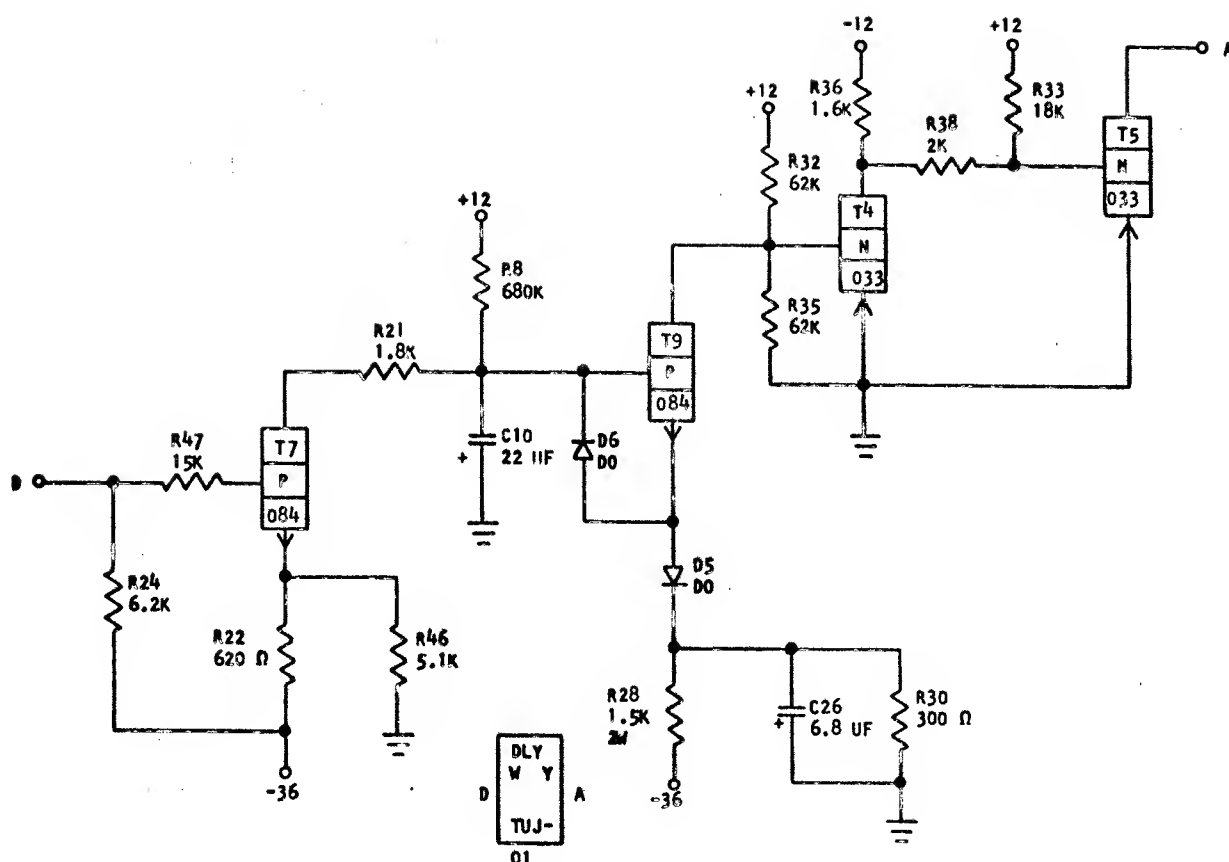
1311

TUH



372580 REF

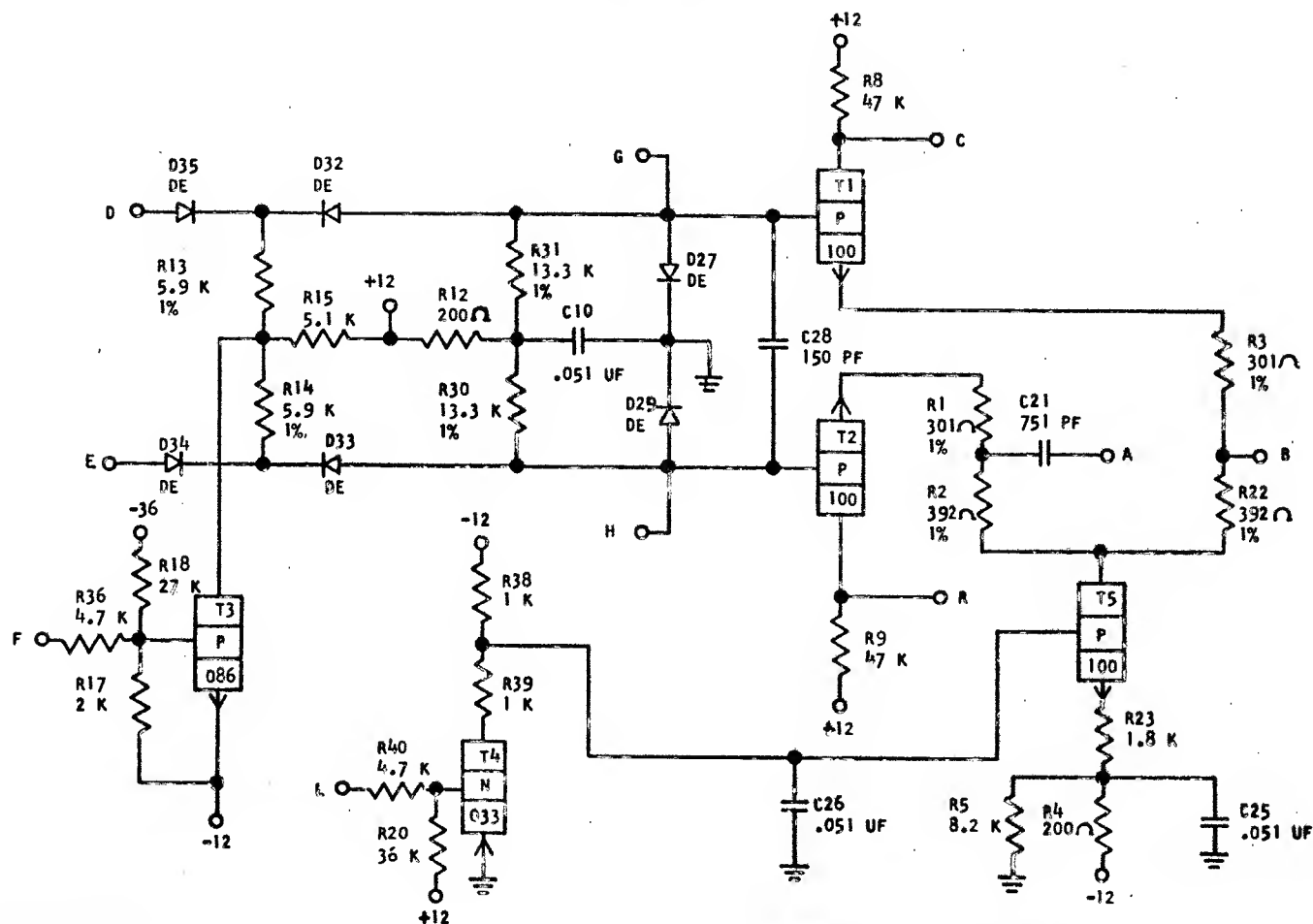
TUJ-



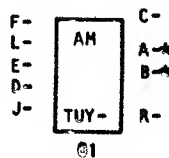
372598 REF

PRE-AMP NOT MOD I

TUY-



372613 REF



* NOYE: PINS A & B ARE JUMPERED TOGETHER ON THE BACK PANEL WHEN THIS CARD IS IN A SATELLITE USED IN A 1440 SYSTEM

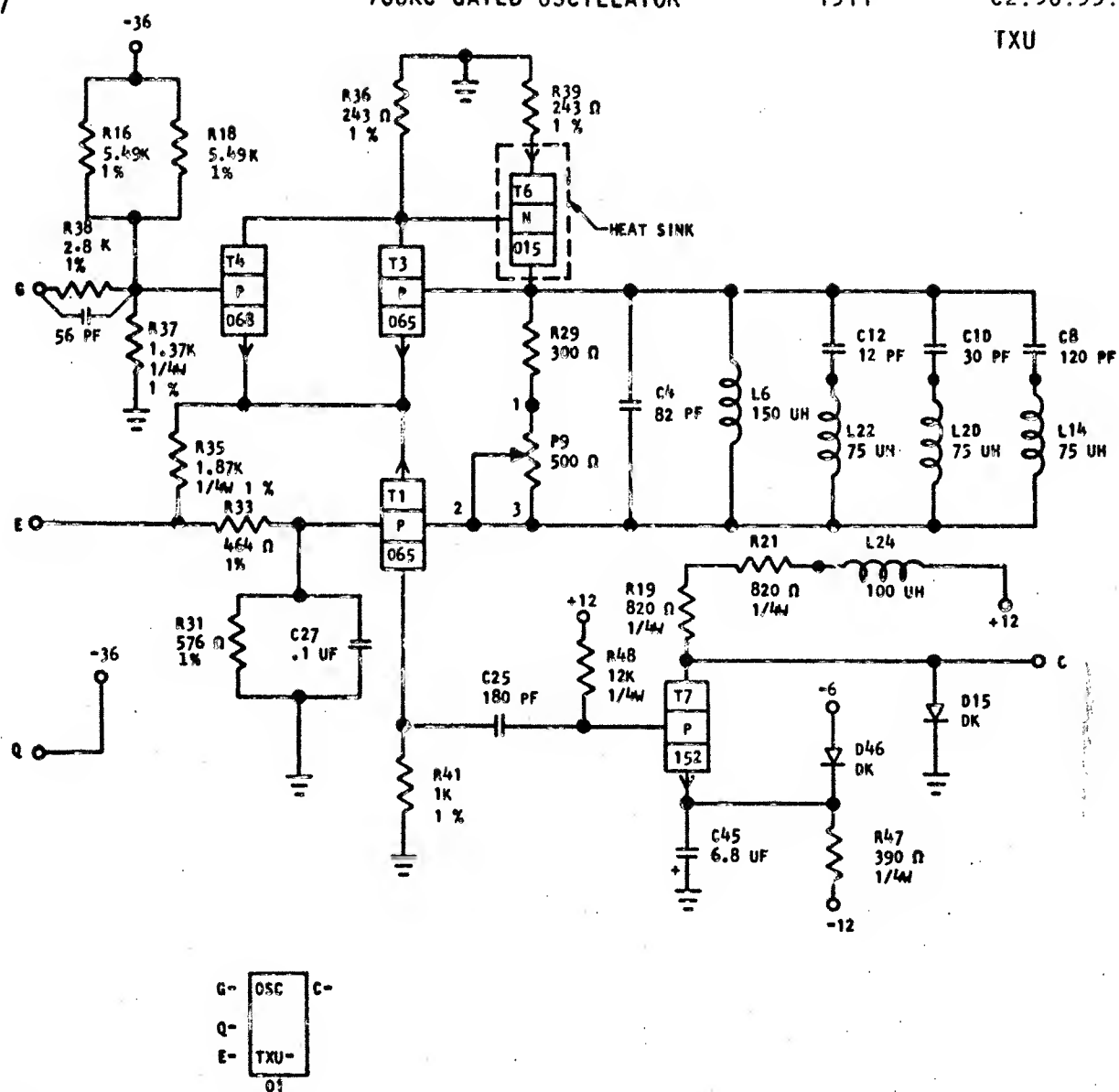
2157397

700KC GATED OSCILLATOR

1311

C2.90.33.9

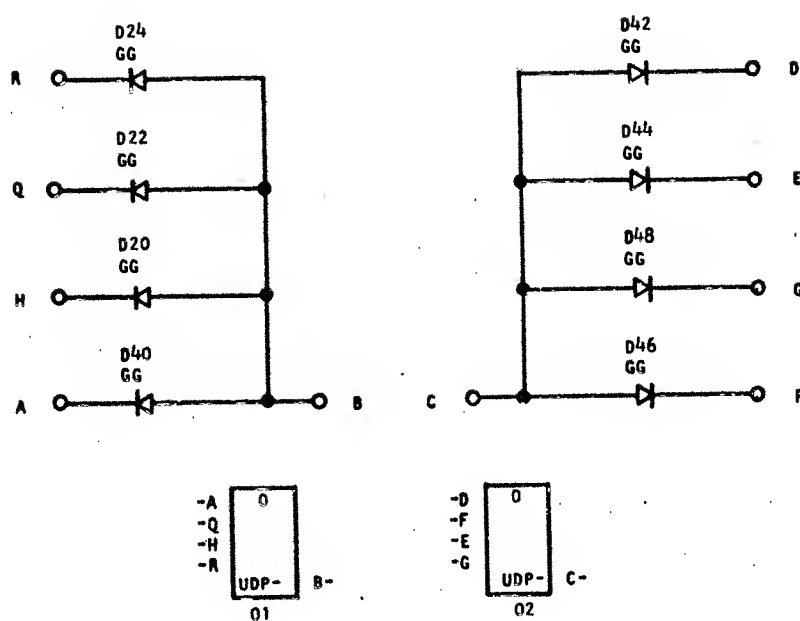
TXU



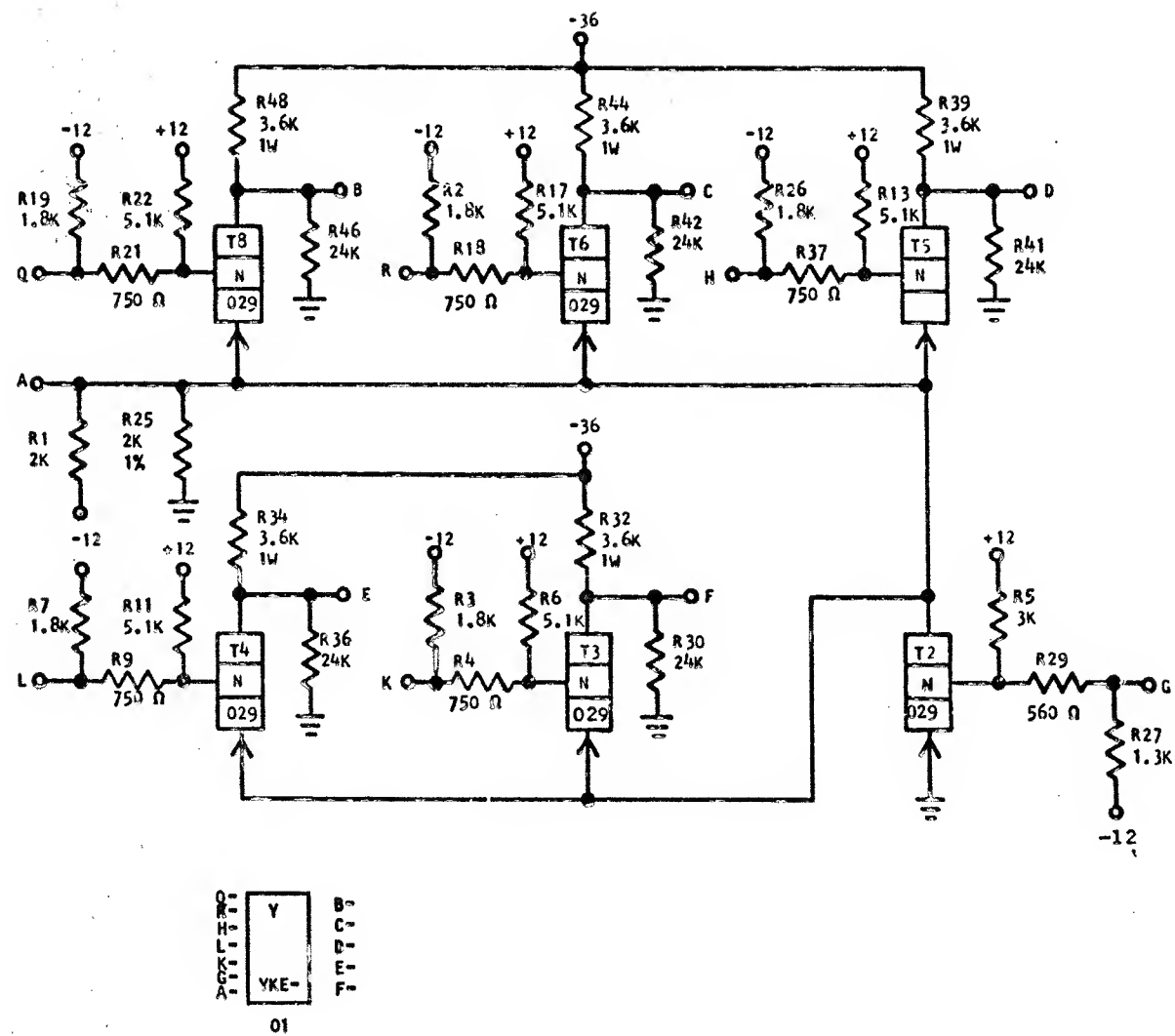
372039 REF

PREAMP GATE #2

UDP



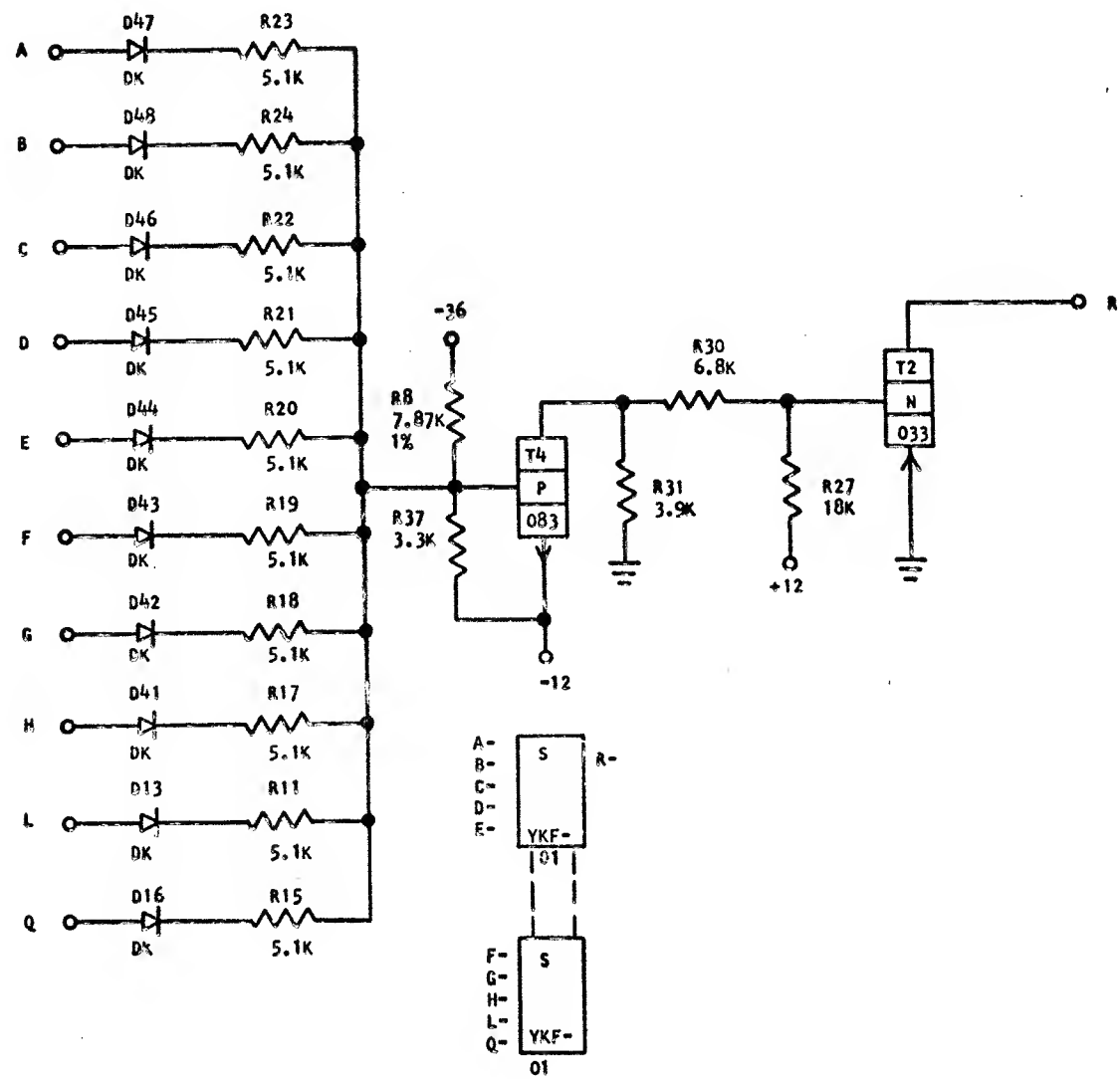
372075 REF



372317 REF

SELECTION SAFETY

YKF



372306 REF

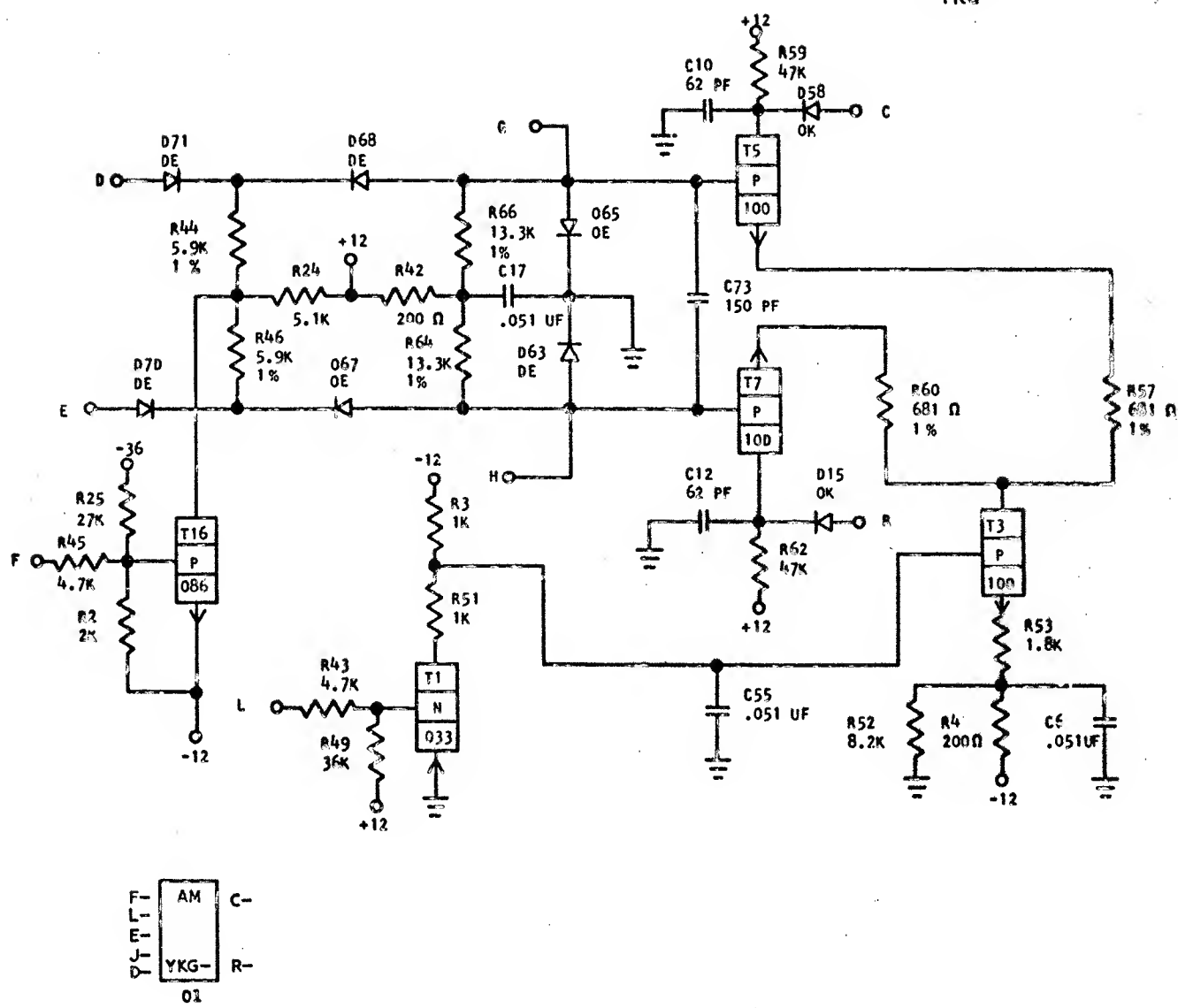
2157235

PREAMP MOD 1

1311

C2.90.35.0

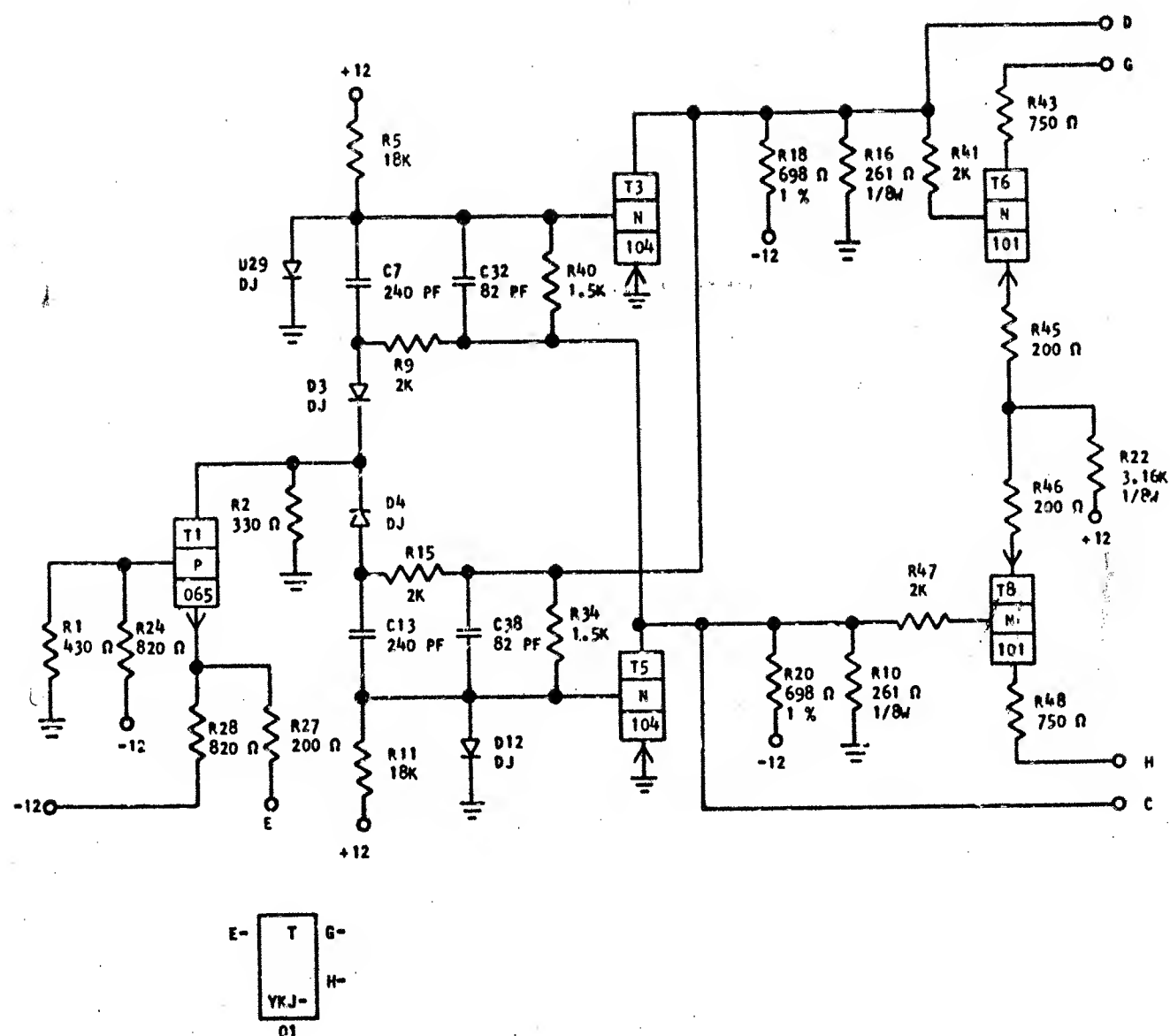
YKG



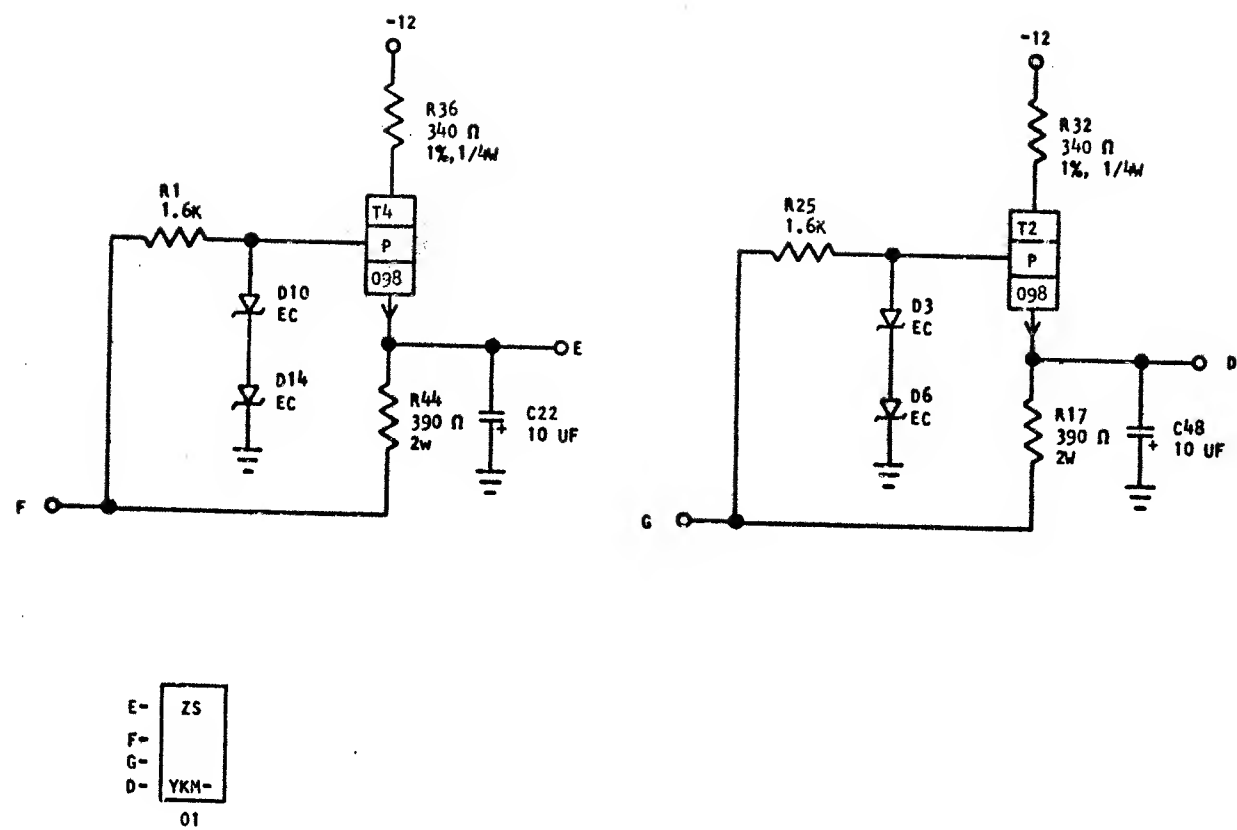
372300 REF

C2.90.36.0

YKJ



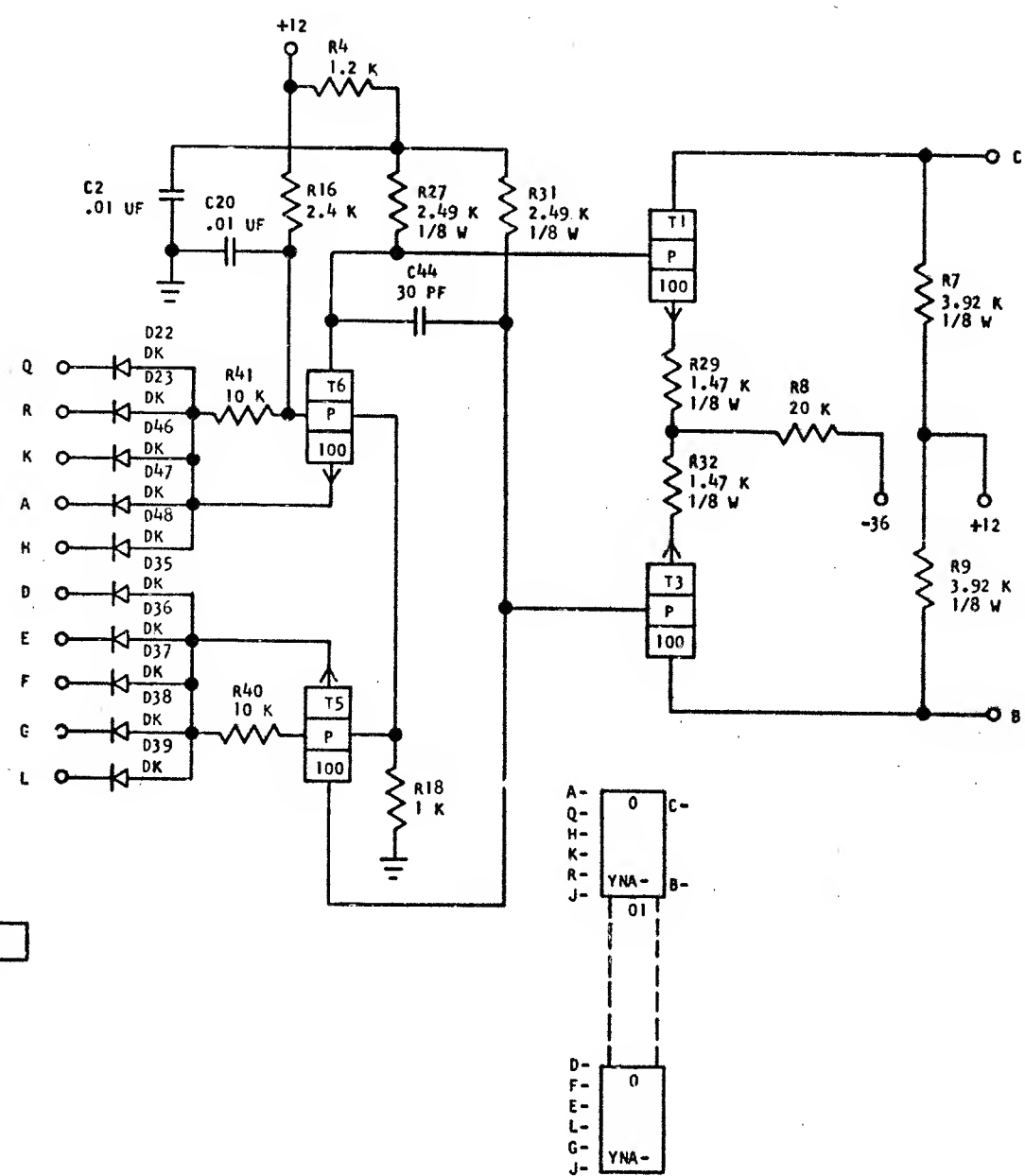
372304 REF



372307 REF

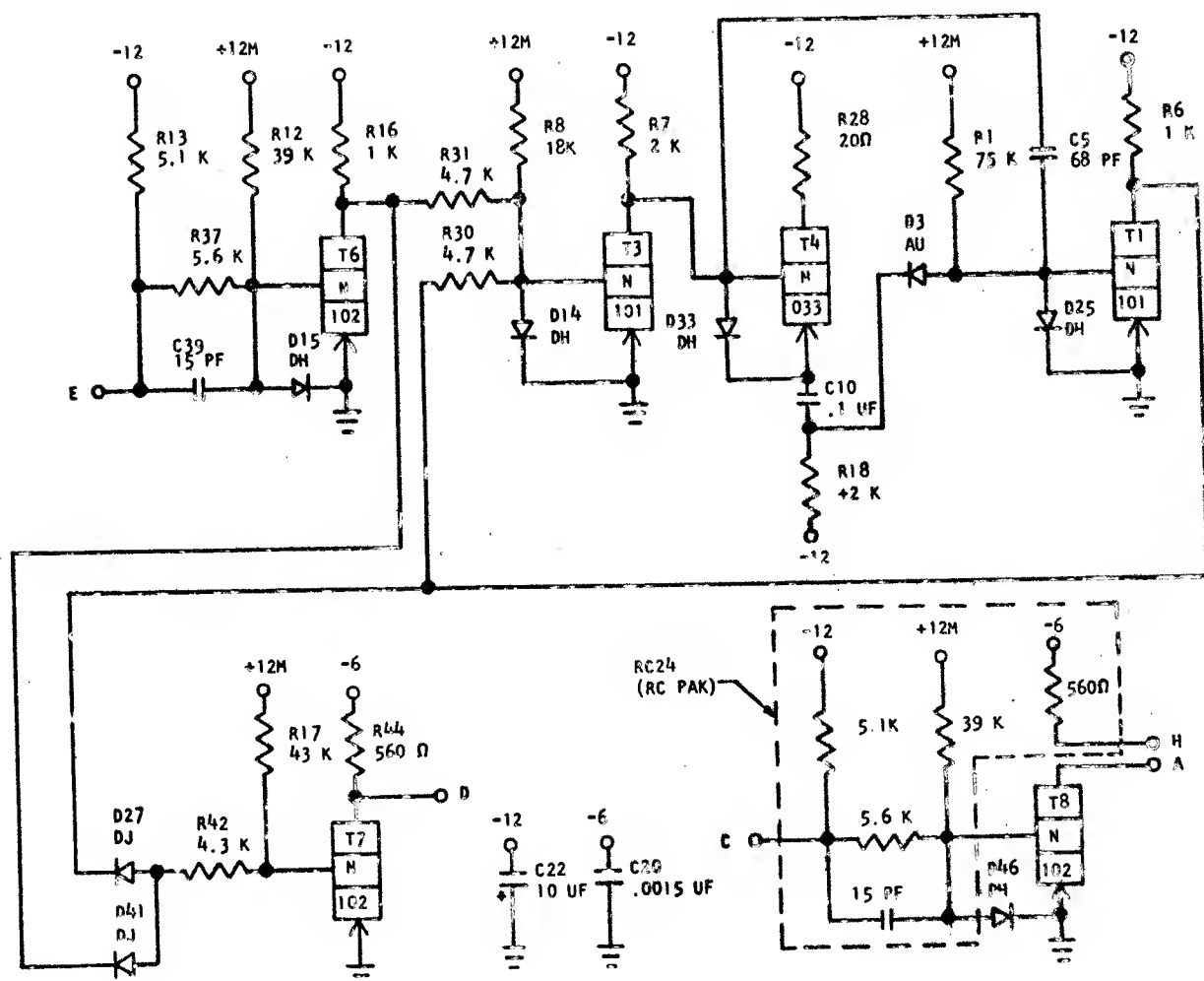
MASTER PRE-AMP GATE

YNA-

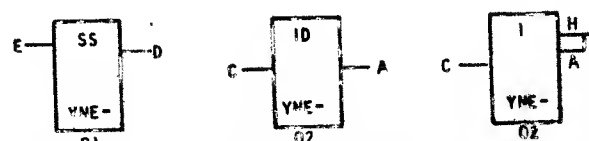


372612 REF

YNE-

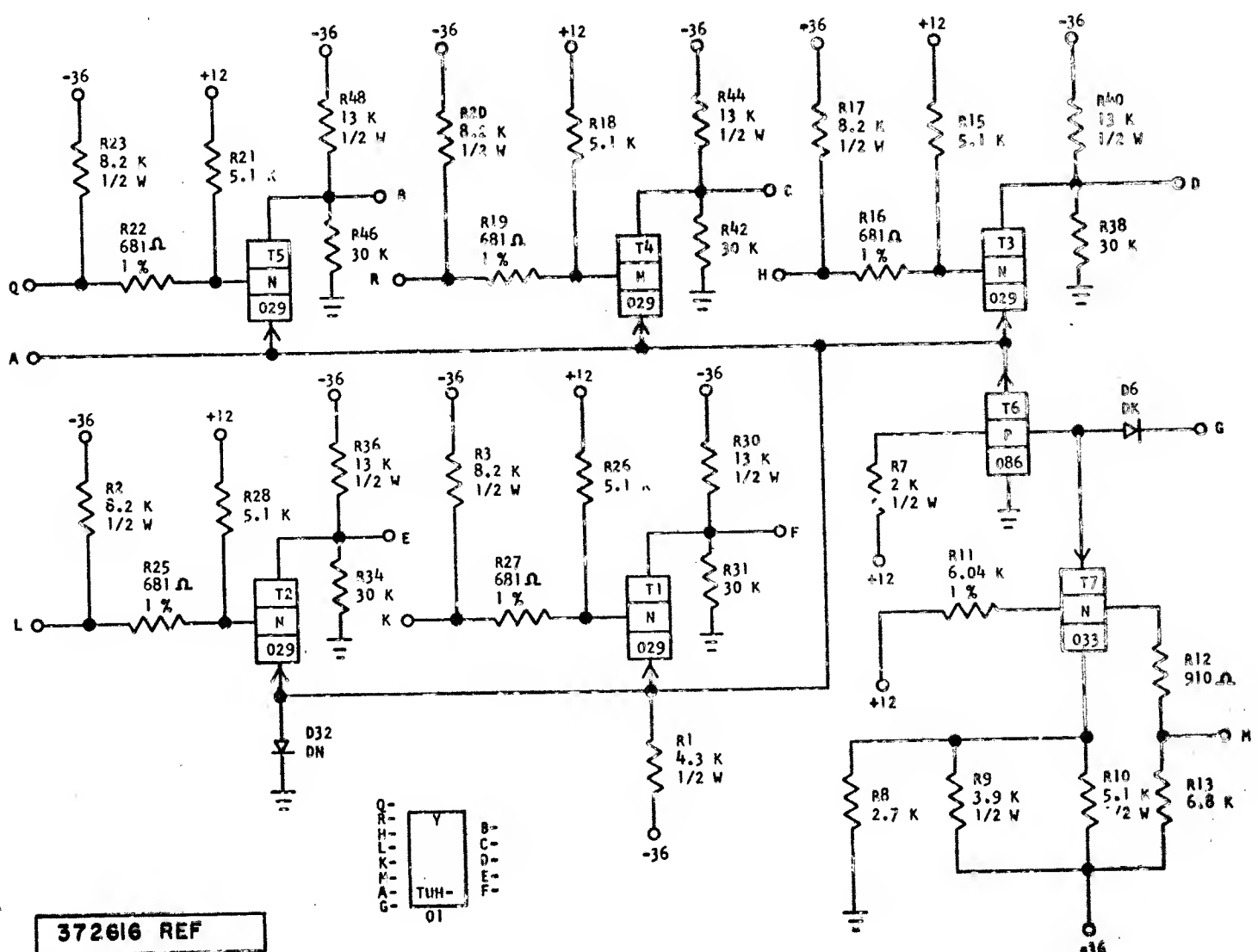


372614 REF

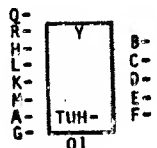


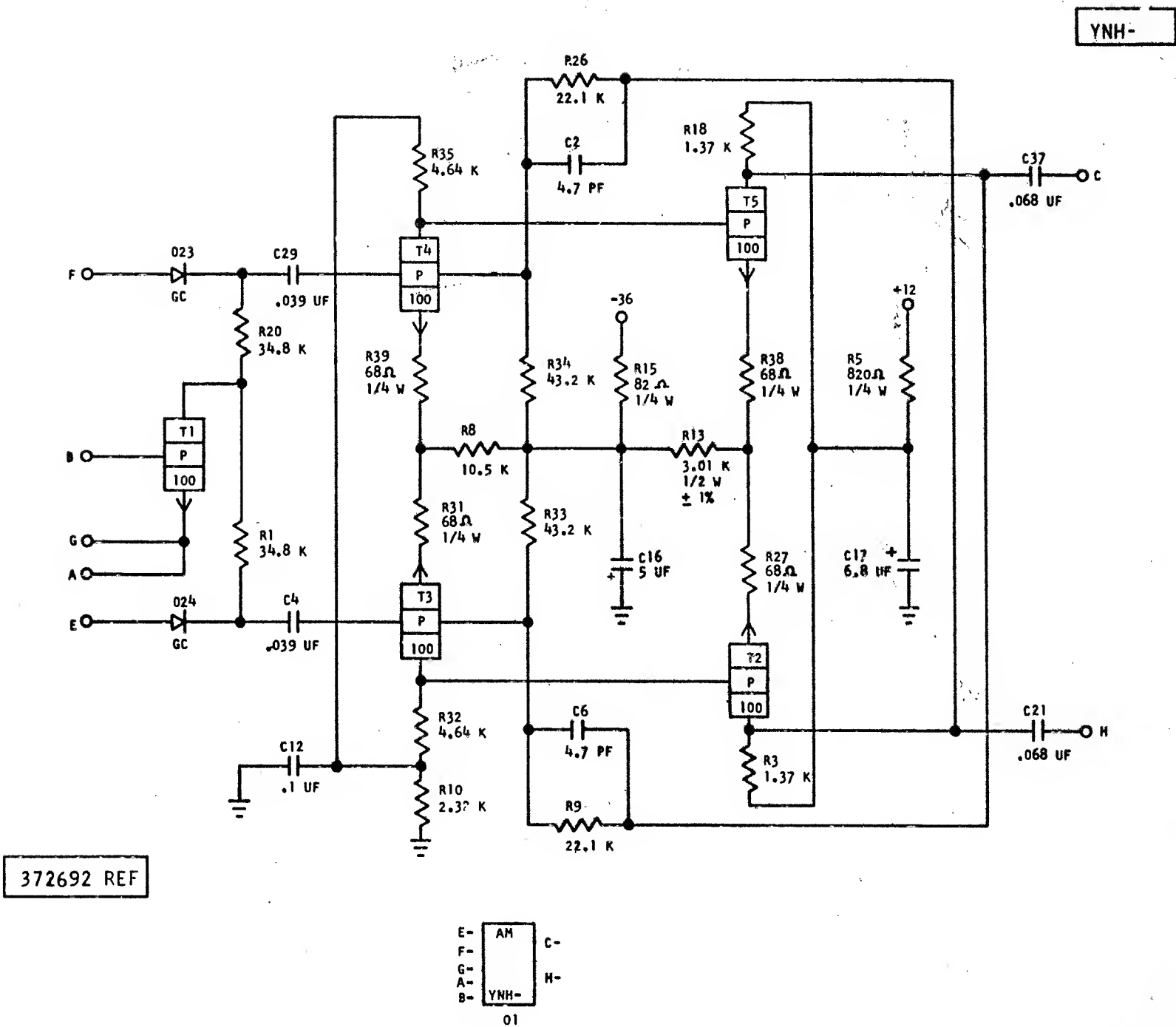
Y-SELECT #1

YNF-

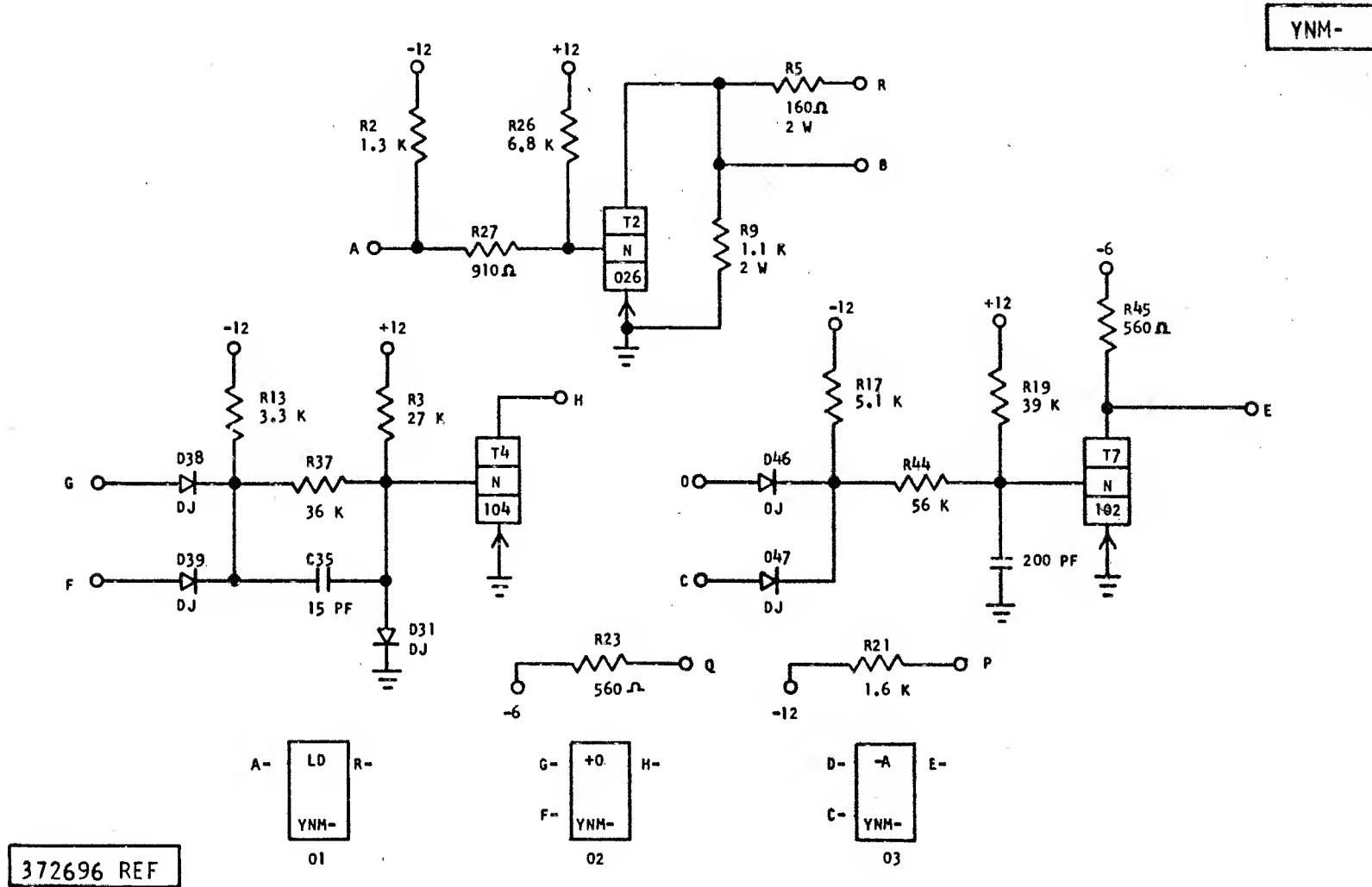


372616 REF

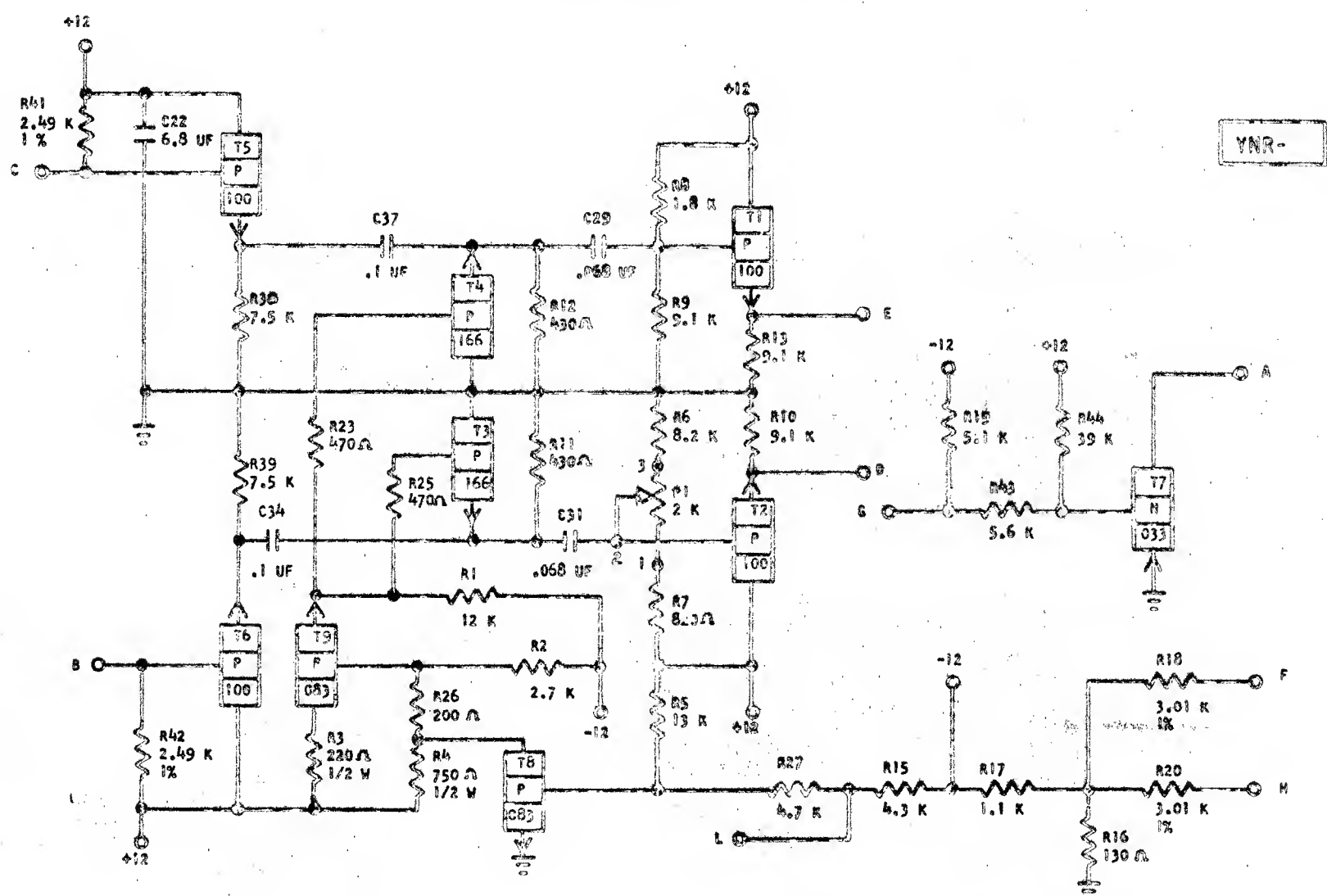




LAMP DRIVERS



BLOCKING CIRCUIT



C- AM D-
B- YNR-01
L- YNR-01

A YNR-02
M- YNR-02

G- 10 A-
YNR-03

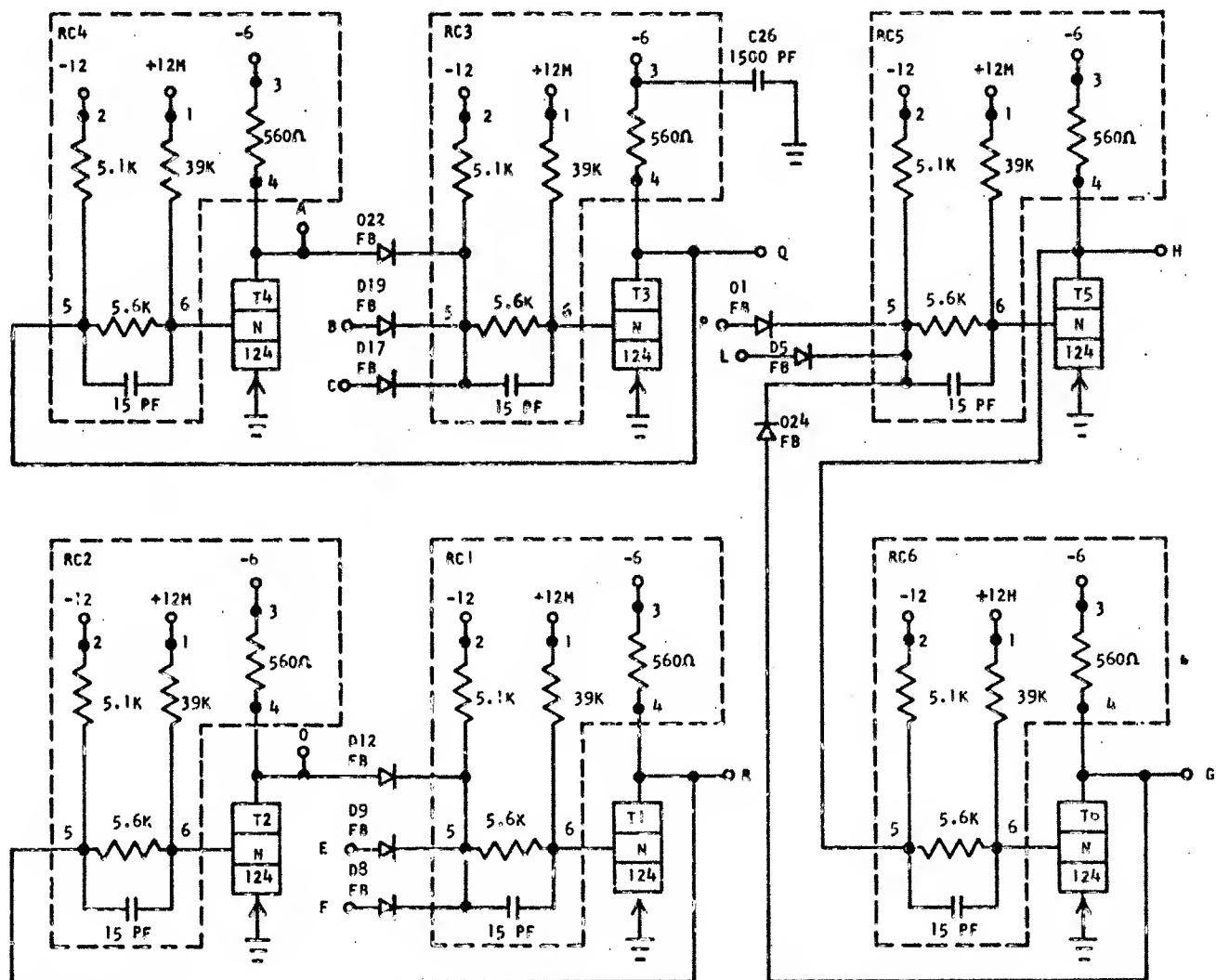
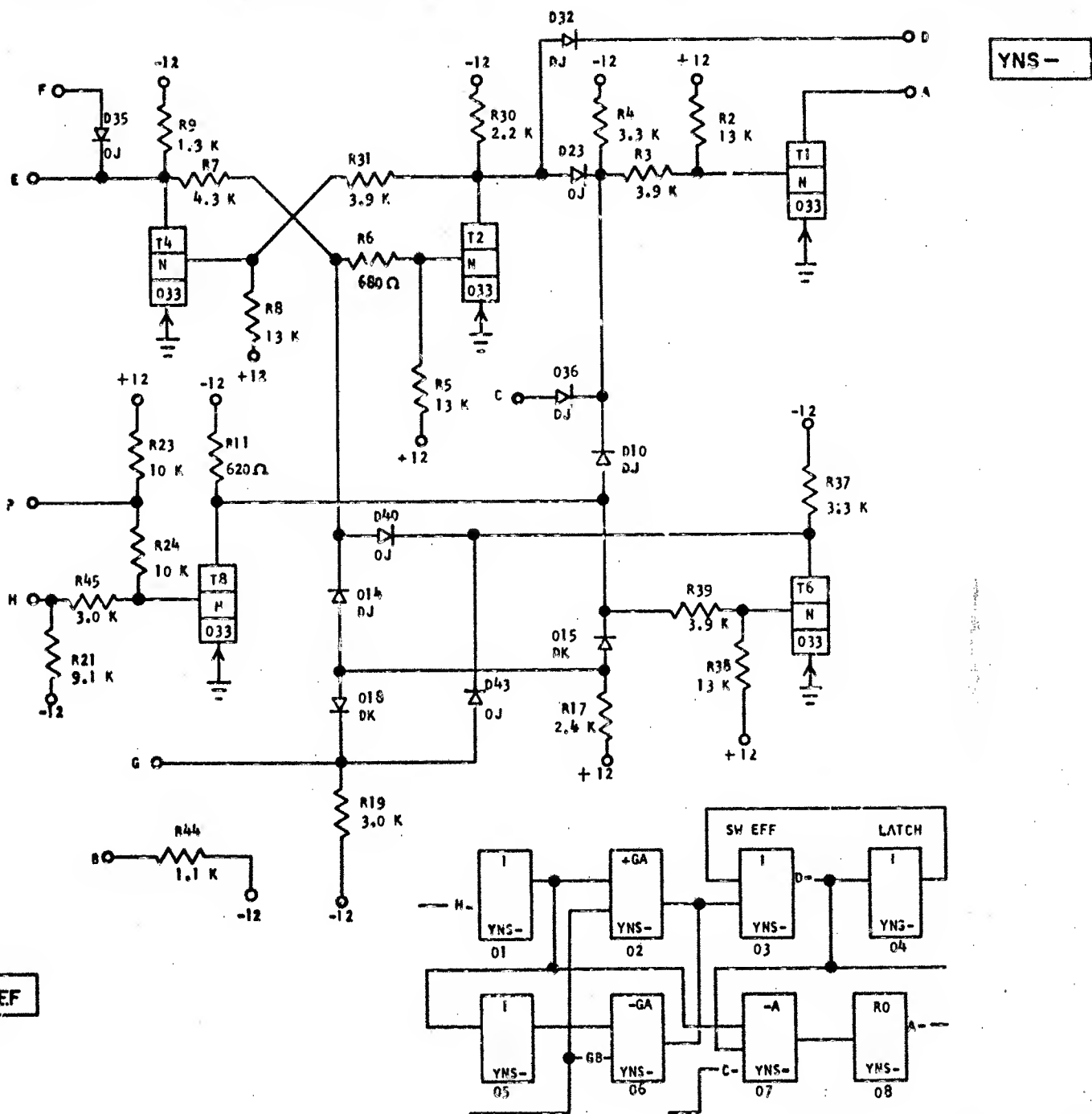
372691 REF

2157281

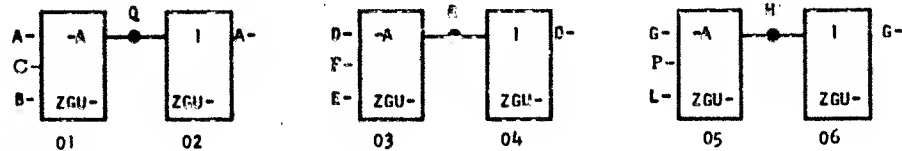
METER CONTROL #1

1311

C2.90.39.0



372603 REF

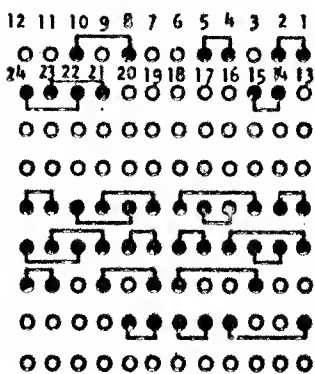


EC 408317

DA 0A22000

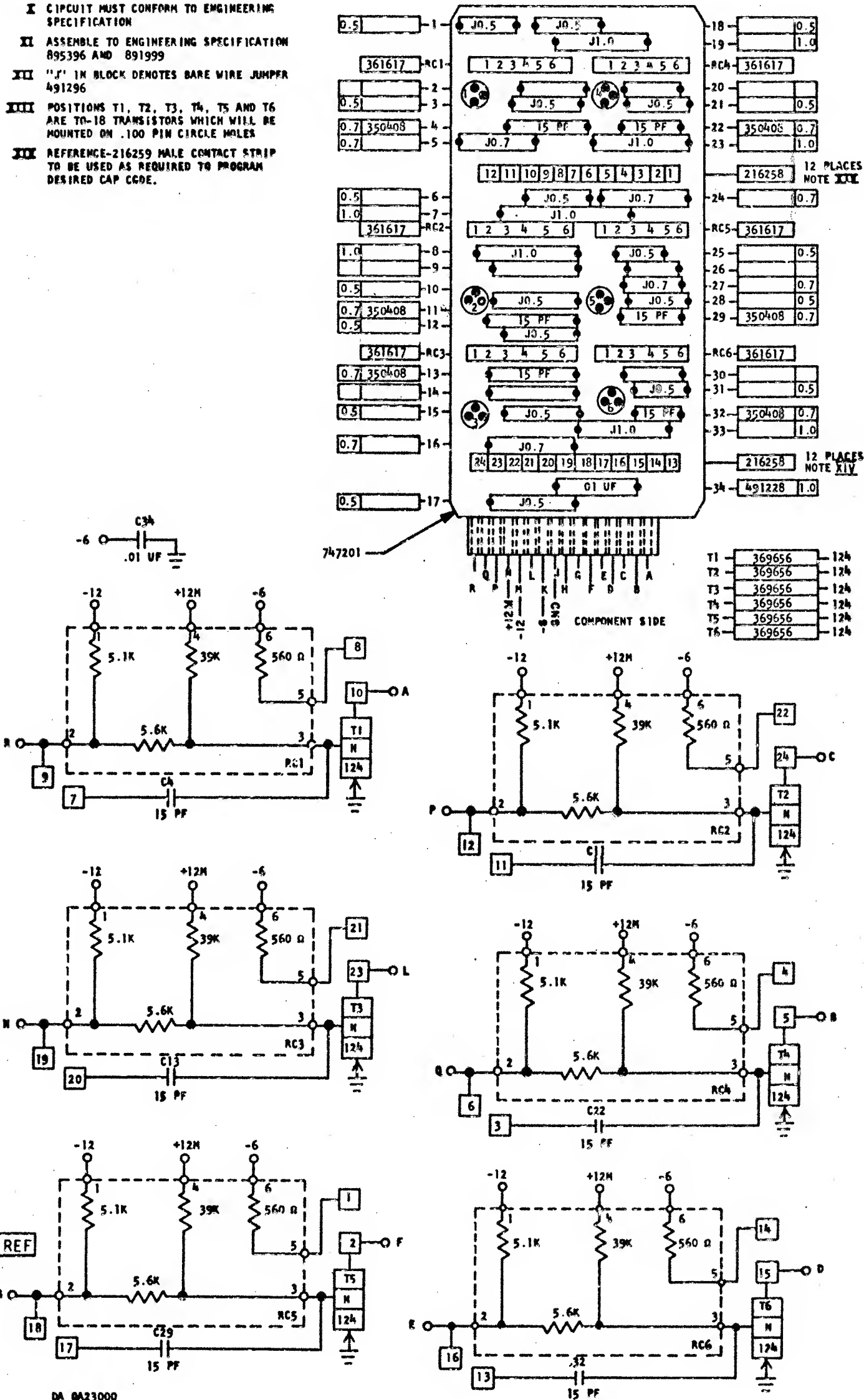
CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC	CARD CODE
INVERTER LOW SPEED WITH LOAD	JR	370348	892380	DHE-
INVERTER LOW SPEED WITHOUT LOAD	--	370372	892380	DHC-
H.S. LOGIC INVERTER	JS	372592	870585	Z6M-
H.S. LOGIC INVERTER WITHOUT LOAD	JT	372593	870585	Z6Q-

CAP CONFIGURATION

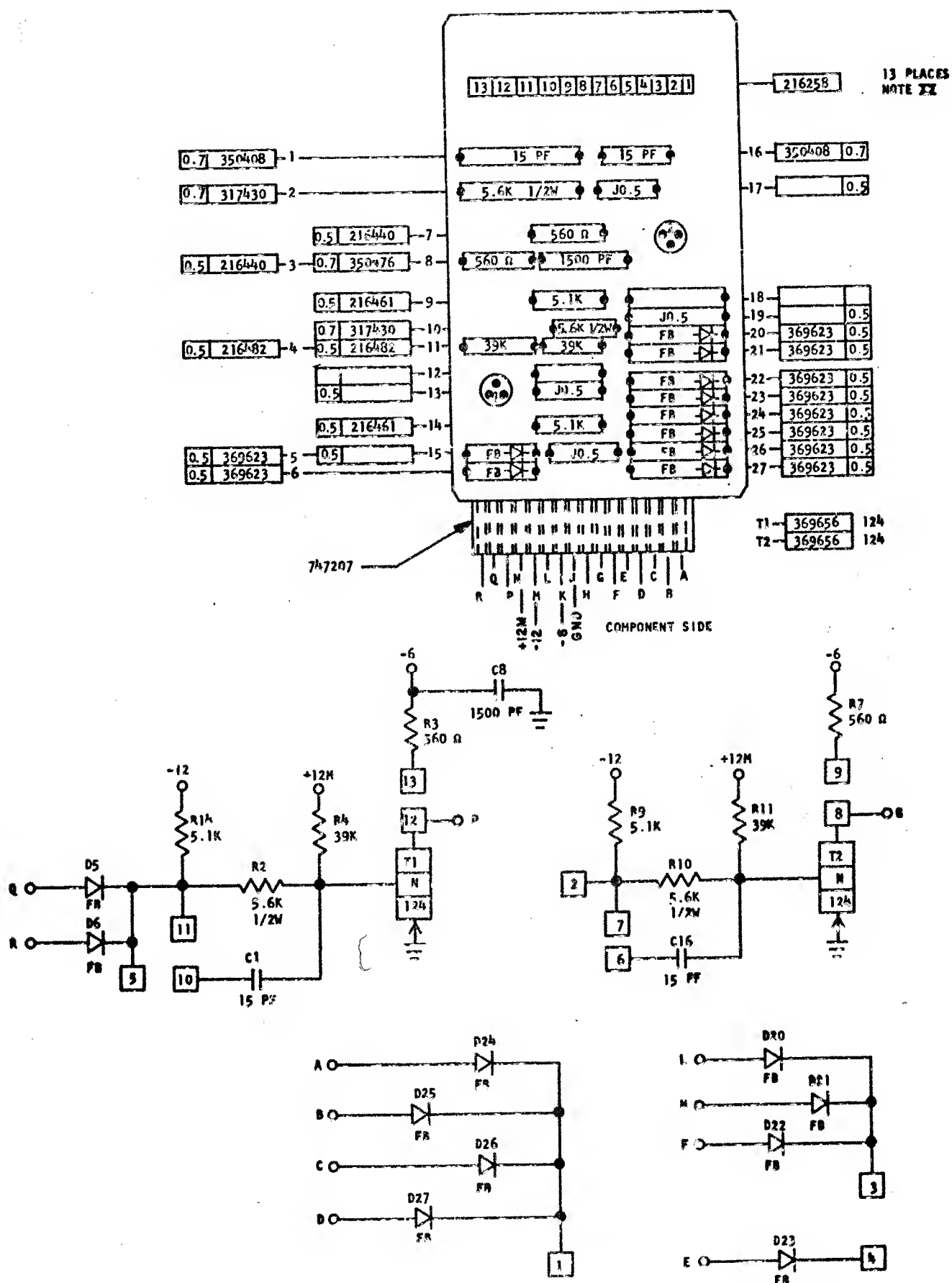


NOTES:

- I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII "J" IN BLOCK DENOTES BARE WIRE JUMPER 491296
- XIII POSITIONS T1, T2, T3, T4, T5 AND T6 ARE TO-18 TRANSISTORS WHICH WILL BE MOUNTED ON .100 PIN CIRCLE HOLES
- XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE.



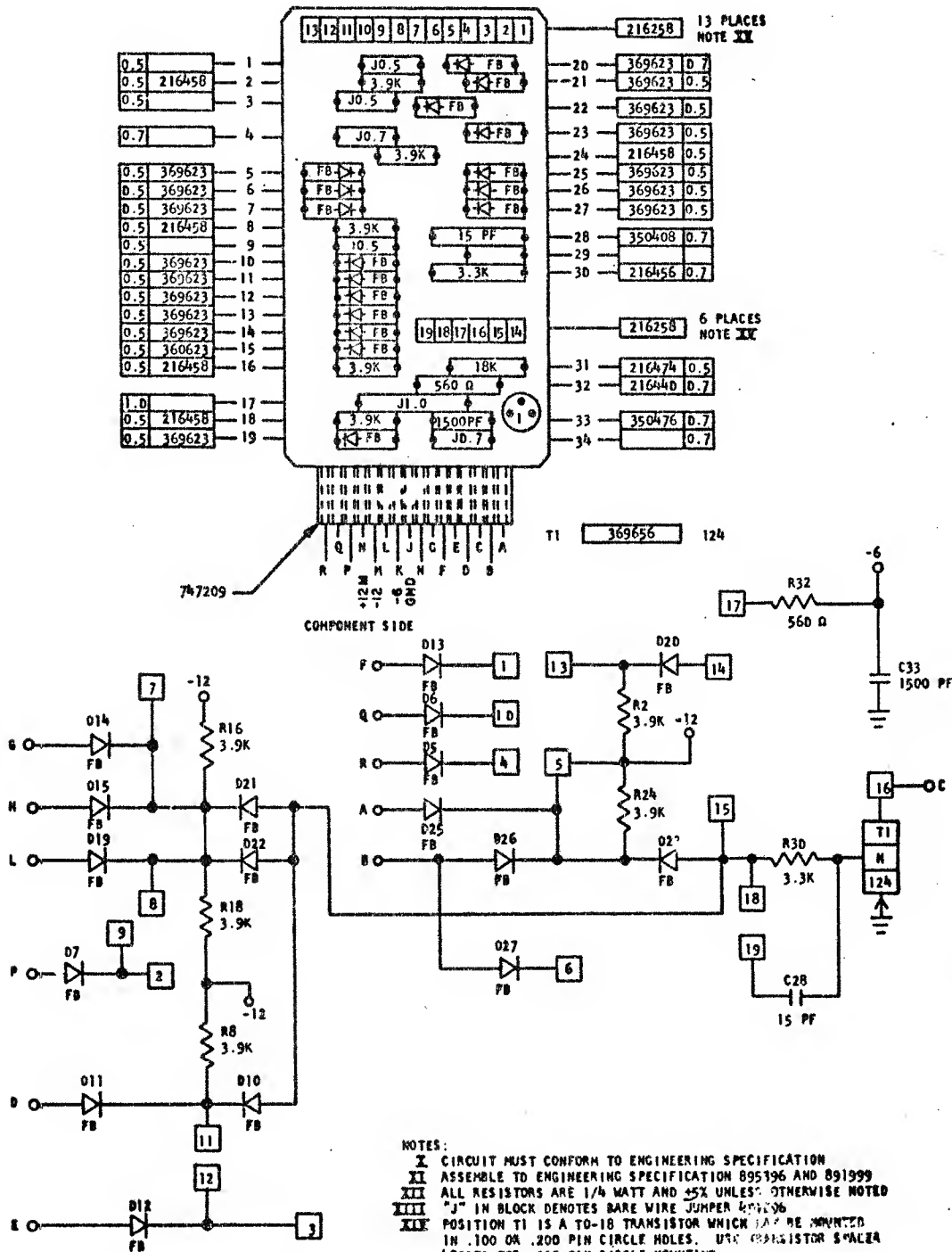
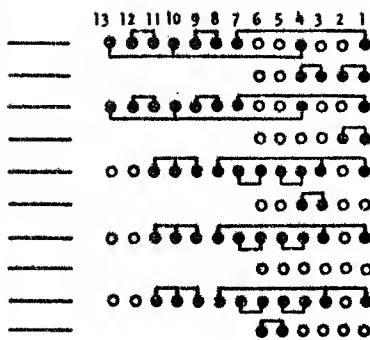
CIRCUIT NAME	CAP CODE	ASM NO.	TEST SPEC	CARD CODE	CAP CONFIGURATION
2-5 WAY (-A) LOADS	KM	372589	870885	ZGL-	13 12 11 10 9 8 7 6 5 4 3 2 1
2-5 WAY (-A) WITHOUT LOADS	KE	372590		ZGM-	
1-10 WAY (-A)	KM	372591	870885	ZSM-	
5 WAY LOGIC BLOCK LOW SPEED W/O LOAD	KG	370375	892380	DGM-	
5 WAY LOGIC BLOCK LOW SPEED W/LOAD	KF	370376	892380	DGX-	
1-6 WAY, 1-4 WAY W/O LOAD (-A)	FL	372123	892216	DMY-	
1-8 WAY AND 1-2 WAY W/O LOAD	KC	372193	892216	DMY-	
1-8 WAY, 1-2 WAY W/LOAD	KJ	372194	892380	DMZ-	
1-6 WAY, 1-4 WAY W/LOAD (-A)	PK	372195	892380	DEM-	
1-6 WAY 1-4 WAY (-A) W/O LOAD N.S.	KD	372528	892216	DMY-	



370953 REF.

CIRCUIT NAME	CAP CODE	ASM. NO.	TEST SPEC	CARD CODE
4-2 WAY, 1-3 WAY (-A,-O)	KN	372207	870201	AXN-
4-2 WAY, 1-3 WAY (-A,-O) WO/LOAD	KP	372213	870201	AXP-
4-3 WAY (-A,-O) W/LOAD - SDTDL	KQ	372214	870201	AXQ-
4-3 WAY (-A,-O) WO/LOAD - SDTDL	KR	372236	870201	AXW-
4-3 WAY (-A,-O) WO/LOAD N.S.	KS	372527	870529	DKX-

CAP CONFIGURATION



370954 REF